TAB 24

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United States Patent File History

Tab Listings

A. References (if applicable)
- **A1**–U.S. References
- **A2**–Foreign References

B. Jacket (face of file, contents flap, index of claims, PTO 270, searched)

C. Printed Patent

D. Specification (serial no. Sheet, abstract, specification, claims)

E. Oath
- **E1**–Small Entity Status (if applicable)

F. Drawing Figures (if applicable)

G. USPTO/Applicant Correspondence

H. Original Patent Application (in cases of FWC)

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Jc526 U.S. PTO 09/097076 06/12/98

ISSUE CLASSIFICATION	Class	Subclass
	716	9

[redacted]

PATENT NUMBER 6192508

6192508

U.S. UTILITY PATENT APPLICATION

O.I.P.E.	PATENT DATE
SCANNED ____ Q.A. ____	FEB 2 0 2001

SECTOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
	716	9		

FILED WITH: ☐ DISK (CRF) ☐ FICHE
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PREPARED AND APPROVED FOR ISSUE

ISSUING CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)						
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					
716	9	716	10	13				
INTERNATIONAL CLASSIFICATION								
G06F 17/50								
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☐ TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
	~~5~~ 1	12	2	18	1
☐ a) The term of this patent subsequent to ____ (date) has been disclaimed.	Dr. Hugh Jones 1/25/00 (Assistant Examiner) (Date)			NOTICE OF ALLOWANCE MAILED	
☐ b) The term of this patent shall not extend beyond the expiration date of U.S Patent. No. ____	KEVIN J. TESKA SUPERVISORY PATENT EXAMINER 1/28/00 (Primary Examiner) (Date)			1-31-00	
				ISSUE FEE	
				Amount Due 605.00	Date Paid 2-16-00
☐ c) The terminal ____ months of this patent have been disclaimed.	Peggy Hamad 2-28-00 (Legal Instruments Examiner) (Date)			ISSUE BATCH NUMBER H-44	

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Form PTO-436A
(Rev. 10/97)

(LABEL AREA) Portal Drawings (1 shts) sp

(FACE)

A-353

PATENT APPLICATION

09097076

Jc52r U.S. PTO
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INITIALS: _____

CONTENTS

	Date received (Incl. C. of M.) or Date Mailed		Date received (Incl. C. of M.) or Date Mailed
1. Application 5 papers.		42.	
2.		43.	
3. Notice of Missing Parts	9-29-98	44.	
4. CFR	8-20-98	45.	
5. CFR	12/14/98	46.	
6. Rejection 3 mos.	11-15-99	47.	
7. Letter Response [illegible]	1-21-00	48.	
8. Notice of Allowability	2-31-00	49.	
9. Cmplt. Cl Rule 312	4-18-00	50.	
10. Letter of Extension	5-9-00	51.	
[redacted]		52.	
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13. Formal Drawing	11-22-00	54.	
14. Drawing Clrx	12-8-00	55.	
~~15. Formal Drawings (4 sheets) set~~	12-8-00	56.	
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ISSUE SLIP STAPLE AREA (for additional cross references)

POSITION	INITIALS	ID NO.	DATE
FEE DETERMINATION	[illegible]	7105	6.17.98
O.I.P.E. CLASSIFIER			
FORMALITY REVIEW			

INDEX OF CLAIMS

✔ ..... Rejected
= ..... Allowed
— (Through numeral) Canceled
÷ ..... Restricted
N ..... Non-elected
I ..... Interference
A ..... Appeal
O ..... Objected

Claim Final	Claim Original	Date
1	(1)	11/3/98
2	2	11/25/98
3	3	
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If more than 150 claims or 10 actions staple additional sheet here

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SEARCHED

Class	Sub.	Date	Exmr.
395	500,1	11/3/99	[illegible]
716	9	1/25/00	[illegible]
716	10	1/25/00	[illegible]
716	13	1/25/00	[illegible]

SEARCH NOTES
(INCLUDING SEARCH STRATEGY)

	Date	Exmr.
East	11/2/99	[illegible]
East	1/25/00	[illegible]

INTERFERENCE SEARCHED

Class	Sub.	Date	Exmr.
716	9	1/25/00	[illegible]
716	10	1/25/00	[illegible]
716	13	1/25/00	[illegible]

(RIGHT OUTSIDE)

US006192508B1

(12) **United States Patent**
Malik et al.

(10) **Patent No.: US 6,192,508 B1**
(45) **Date of Patent: Feb. 20, 2001**

(54) **METHOD FOR LOGIC OPTIMIZATION FOR IMPROVING TIMING AND CONGESTION DURING PLACEMENT IN INTEGRATED CIRCUIT DESIGN**

(75) Inventors: **Sharad Malik**, Princeton, NJ (US); **Lawrence Pileggi**, Pittsburgh, PA (US); **Abhijeet Chakraborty**, Sunnyvale, CA (US); **Gary K. Yeap**, San Jose, CA (US); **Douglas B. Boyle**, Palo Alto, CA (US)

(73) Assignee: **Monterey Design Systems**, Sunneyvale, CA (US)

(*) Notice: Under 35 U.S.C. 154(b), the term of this patent shall be extended for 0 days.

(21) Appl. No.: **09/097,076**

(22) Filed: **Jun. 12, 1998**

(51) **Int. Cl.**[7] **G06F 17/50**
(52) **U.S. Cl.** **716/9**; 716/10; 716/13
(58) **Field of Search** 395/500.1; 716/9, 716/10, 13

(56) **References Cited**

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4,484,292 * 11/1984 Hong et al. 716/13
5,557,533 * 9/1996 Koford et al. 706/13
5,561,772 * 10/1996 Dorner et al. 710/101
5,572,482 * 11/1996 Hoshizaki et al. 365/233
5,847,965 * 12/1998 Cheng 395/500.09

* cited by examiner

Primary Examiner—Kevin J. Teska
Assistant Examiner—Hugh Jones
(74) *Attorney, Agent, or Firm*—Burns Doane Swecker & Mathis L.L.P

(57) **ABSTRACT**

This invention recognizes the ability of logic optimization to help placement relieve congestion. Different types of logic optimizations are used to help placement relieve congestion. In one type of optimization, the speed of parts of the circuit is improved by selecting faster cells. In another type of optimization, the topology of the circuit is changed such that placement can now move cells, which could not have been moved before, to reduce congestion and thus enable routing. A distinguishing feature of this methodology is that it not only uses the placement information for interconnection delay/area estimates during logic optimization, but also uses logic optimization to aid the physical placement steps by providing support to placement so that the congestion of the circuit is improved. The aim is to avoid getting into a situation where the placed circuit cannot be routed.

18 Claims, 4 Drawing Sheets

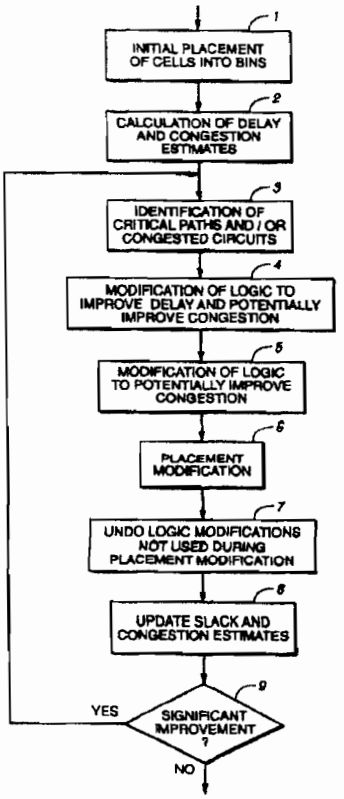
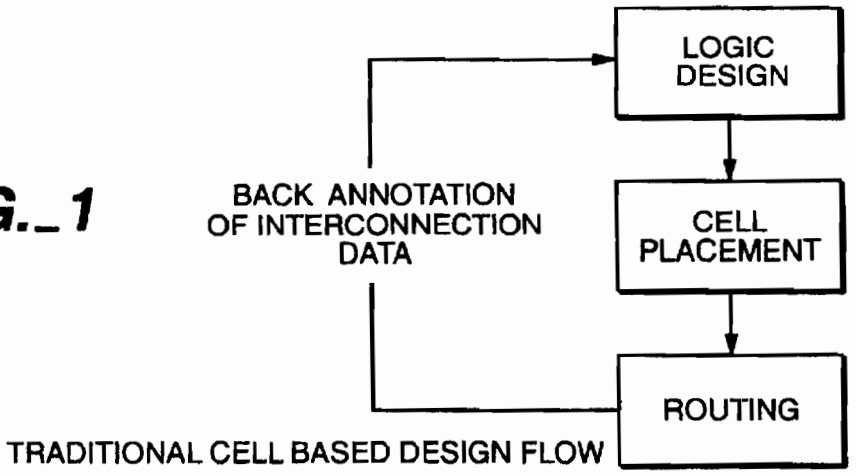
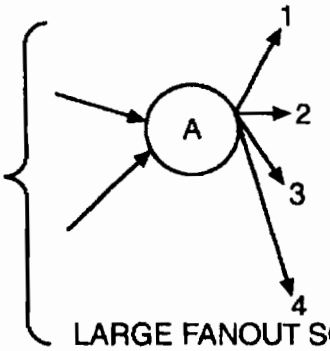


FIG._1



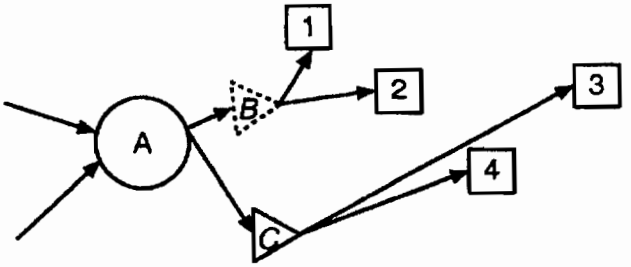
TRADITIONAL CELL BASED DESIGN FLOW

FIG._3A



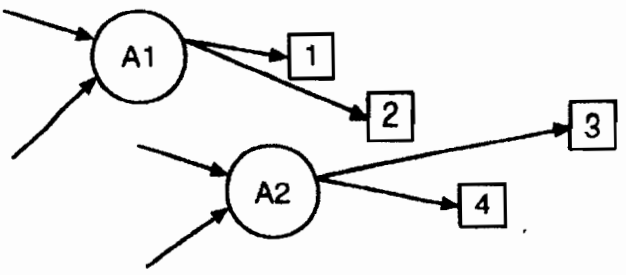
LARGE FANOUT SOURCE OF CONGESTION

FIG._3B



FANOUT SPLITTING USING BUFFERING

FIG._3C



FANOUT SPLITTING USING NODE SPLITTING

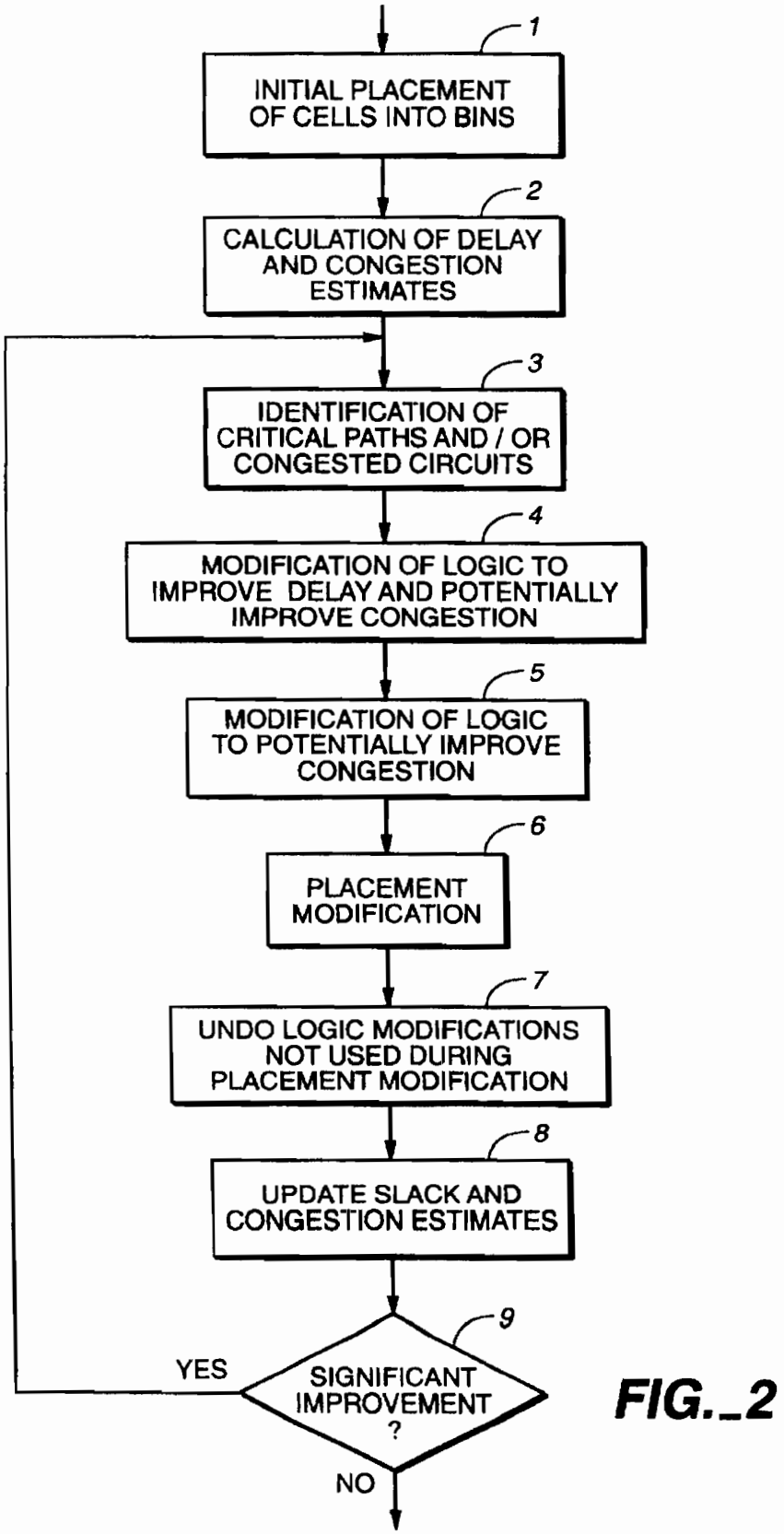
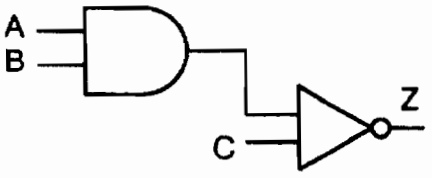

1
INITIAL PLACEMENT OF CELLS INTO BINS
2
CALCULATION OF DELAY AND CONGESTION ESTIMATES
3
IDENTIFICATION OF CRITICAL PATHS AND / OR CONGESTED CIRCUITS
4
MODIFICATION OF LOGIC TO IMPROVE DELAY AND POTENTIALLY IMPROVE CONGESTION
5
MODIFICATION OF LOGIC TO POTENTIALLY IMPROVE CONGESTION
6
PLACEMENT MODIFICATION
7
UNDO LOGIC MODIFICATIONS NOT USED DURING PLACEMENT MODIFICATION
8
UPDATE SLACK AND CONGESTION ESTIMATES
9
SIGNIFICANT IMPROVEMENT ?
YES
NO

FIG._2



BOTH GATES ARE IN THE SAME BIN

FIG._4A

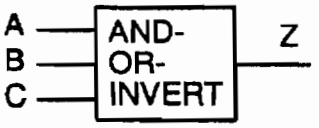


FIG._4B

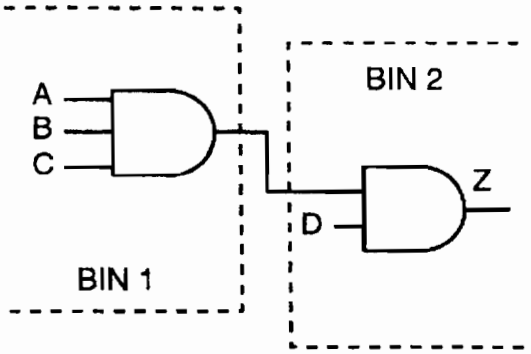


FIG._5A

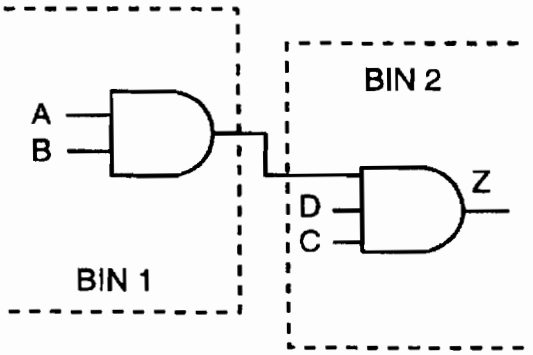


FIG._5B

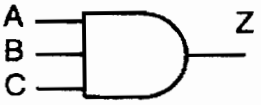


FIG._6A

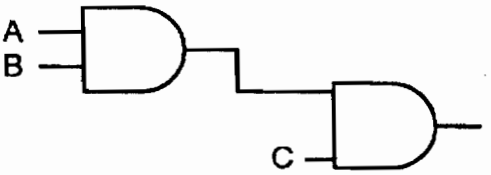


FIG._6B

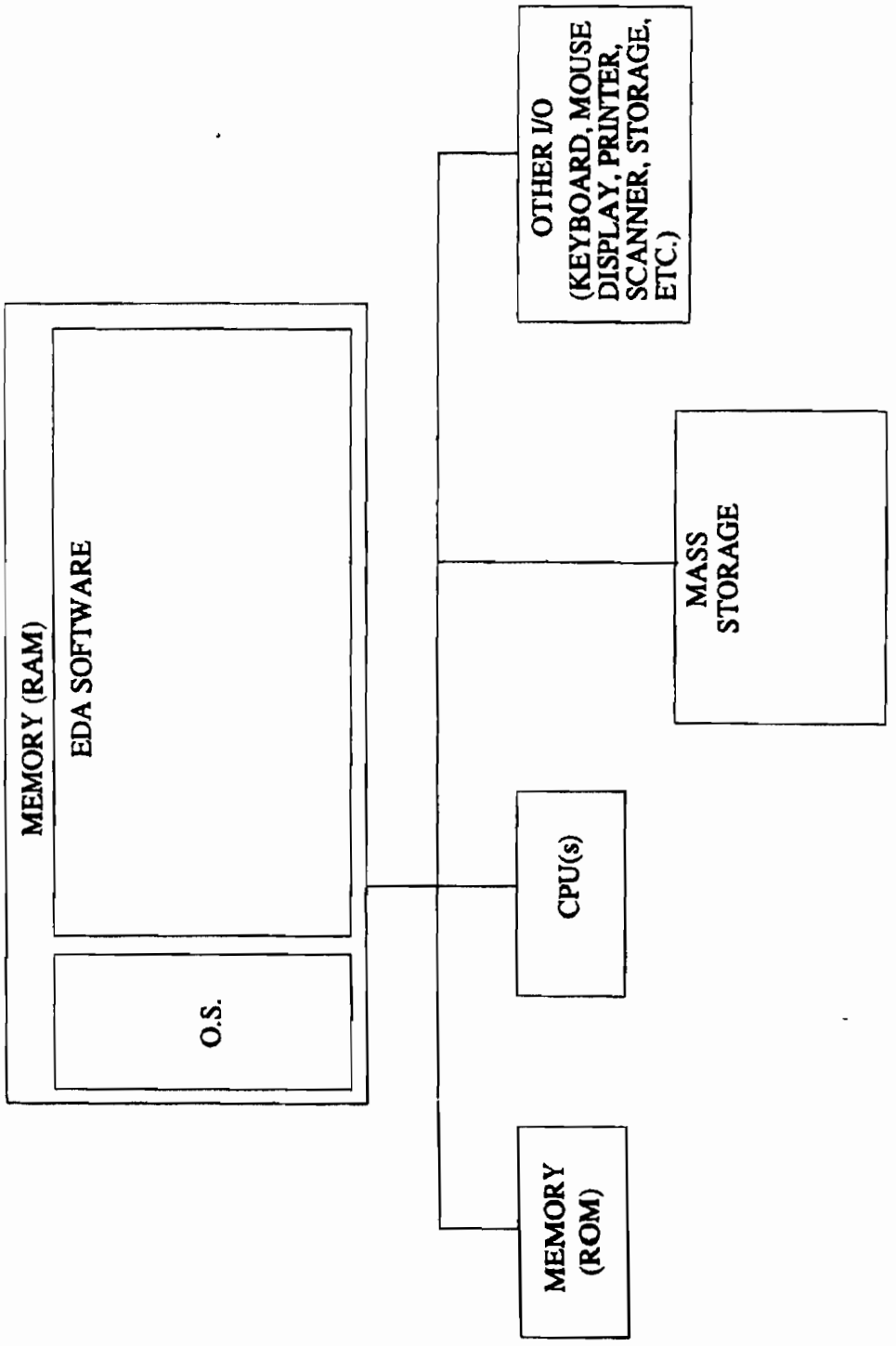

MEMORY (RAM)
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Fig. 7

METHOD FOR LOGIC OPTIMIZATION FOR IMPROVING TIMING AND CONGESTION DURING PLACEMENT IN INTEGRATED CIRCUIT DESIGN

This application is related by subject matter to U.S. Application Ser. No. 09/097,299 entitled METHOD FOR DESIGN OPTIMIZATION USING LOGICAL AND PHYSICAL INFORMATION, filed on even date herewith and incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to integrated circuit design and layout.

2. State of the Art

Traditional cell-based integrated circuit design follows several steps. The first step is designing the logical gate-level circuit that implements the function to be realized by the circuit (referred to as logic design or logic synthesis, of which logic optimizations are a key part). The next step is placing the gates (or cells) in a physical layout, and the final step is routing the interconnection between the cells. With increasing dominance of interconnection delays and area in circuits implemented in deep submicron technologies, this approach is proving to be no longer viable. The problem is that, during the logic optimization stage, the interconnection is not known yet, and thus the dominant part of the area and the delay cannot be considered.

Attempts to overcome this problem have considered alternating logic synthesis and placement and routing, with "back annotation" of the interconnect information to the subsequent logic synthesis steps. Referring to FIG. 1, showing traditional cell-based design flow, a logic design phase is followed by a cell placement phase and then a routing phase. Following the routing phase, interconnection data is back annotated. The logic design, cell placement and routing phases are then repeated. This cycle is continued until, during the routing phase, the design is successfully routed. The problem with this method is that the logic synthesis steps that consider the back annotation information cannot guarantee to fix problems that prevent routing without introducing additional problems due to the modifications made to the circuit gates and topology. There results a large number of iterations between logic synthesis and subsequent place and route, with the possibility of the process never converging.

An alternative approach is to consider placement information during logic optimization. In this methodology, sometimes termed "placement aware synthesis," placement information is made available in varying degrees during logic optimization, i.e. some placement is done as part of logic synthesis (sometimes referred to in the industry as just synthesis). Logic optimization uses this placement information to estimate the effect of the interconnects on the delay and the area of the circuit. Thus logic optimization attempts to accurately model the interconnect delay and area that might result during a placement step. However, it may result in a placed circuit that cannot be routed using the area resources provided by the placement step. The inability to route the resulting placed circuit results in modifications to the placement, consequently nullifying the interconnection information used during logic optimization.

A circuit that has been placed but cannot be routed subject to the available area constraints is not realizable. Additional routing resources must be created to enable the routing.

There results an increase in circuit area and possibly delay, since the wires may now need to go through longer paths.

Placement algorithms are limited in how they can place cells by the timing constraints placed on the design. The timing constraints may result in certain parts of the design being very congested in terms of the wiring (or interconnection) resources needed to connect the cells in those parts of the circuit. It would be possible to relieve the congestion if somehow the cells in the congested area were to be moved apart. However, moving the cells apart may result in an increase in the interconnection delays, which in turn may result in a violation of the timing constraints. Thus a situation results where it is possible to have acceptable timing slacks or acceptable congestion but not both.

The paper by Villarubia and Hojat (ICCD 97) proposes integrated logic optimization and placement. However, the proposed methodology alternates placement and logic optimization and does not consider the impact of the logic optimizations on subsequent placement steps.

SUMMARY OF THE INVENTION

This invention recognizes the ability of logic optimization to help placement relieve congestion. Different types of logic optimizations are used to help placement relieve congestion. In one type of optimization, the speed of parts of the circuit is improved by selecting faster cells. In another type of optimization, the topology of the circuit is changed such that placement can now move cells, which could not have been moved before, to reduce congestion and thus enable routing. A distinguishing feature of this methodology is that it not only uses the placement information for interconnection delay/area estimates during logic optimization, but also uses logic optimization to aid the physical placement steps by providing support to placement so that the congestion of the circuit is improved. The aim is to avoid getting into a situation where the placed circuit cannot be routed.

There are two specific ways in which logic optimization aids placement in relieving congestion. The first method involves determining parts of the circuit which are congested, and then speeding up the logic in these parts. This speedup provides timing slack for a subsequent placement step to move cells while ensuring that this move does not cause the modified interconnections to violate timing constraints. The second method involves modifying the topology of the circuit by adding gates while maintaining the functionality, such that the added gates can then be moved by the placement steps to relieve congestion.

An important aspect of the optimizations, specifically directed towards helping placement relieve congestion, is the ability to undo modifications if placement does not actually use the modifications. The undo capability ensures that no area/power resources are wasted for transformations that are not used as intended.

A critical problem in using logic optimization as part of placement is that logic optimization steps can and do increase the area of circuits. This increase in area can invalidate the results of any placement done thus far, and consequently result in the inability of the combination of these steps to converge. An important part of this invention is to actively bound the area increase of specific parts of the circuit which guarantees that the current placement results are still valid after the logic optimizations, consequently guaranteeing convergence of the integrated logic optimization and placement steps.

BRIEF DESCRIPTION OF THE DRAWING

The present invention may be further understood from the following description in conjunction with the appended drawing. In the drawing:

FIG. **1** is a flowchart of traditional cell-based design flow;

FIG. **2** is a flowchart of design flow in accordance with the present invention;

FIG. **3**(*a*) is a diagram of a gate having a large fanout;

FIG. **3**(*b*) is a diagram of the gate of FIG. **3**(*a*) following fanout splitting using buffering;

FIG. **3**(*c*) is a diagram of a circuit equivalent to the gate of FIG. **3**(*a*) following fanout splitting using node splitting;

FIG. **4**(*a*) is a diagram of a circuit to which intra-bin pin density logic optimization may be applied;

FIG. **4**(*b*) is a diagram of an equivalent circuit resulting from intra-bin pin density logic optimization applied to the circuit of FIG. **4**(*a*);

FIG. **5**(*a*) is a diagram of a circuit to which inter-bin pin density logic optimization may be applied;

FIG. **5**(*b*) is a diagram of an equivalent circuit resulting from inter-bin pin density logic optimization applied to the circuit of FIG. **5**(*a*);

FIG. **6**(*a*) is a diagram of a circuit to which input splitting logic optimization may be applied;

FIG. **6**(*b*) is a diagram of an equivalent circuit resulting from input splitting logic optimization applied to the circuit of FIG. **6**(*a*);

FIG. **7** is a block diagram of a computer system that may be used to practice the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention may be used in conjunction with an electronic design automation placement tool. In accordance with an exemplary embodiment of one such placement tool, at each stage in cell placement, the cells are partitioned into a number of bins. Interconnection models for interconnects between bins and within bins provide both delay estimates for each interconnect in the circuit, as well as congestion estimates for each bin in the circuit. The circuit has timing constraints imposed on it that it needs to satisfy. The delay estimates of the interconnection, combined with the delays of the cells and the timing constraints imposed on the design, are converted to timing slack information for each part of the circuit. A negative timing slack indicates that that part of the circuit is not meeting the timing constraints. A positive slack indicates that that part of the circuit is producing its result faster than is needed and can thus be slowed down without violating its timing constraints. More generally, "slack" is defined herein as a measure of the degree to which a timing requirement is met in an integrated circuit design.

The traditional role of logic synthesis has been to identify areas of the circuit which have negative timing slack and then modify the circuit so as to fix this problem. As described herein, logic synthesis is used to aid placement to achieve both acceptable delays and congestion, by making circuit modifications that increase the timing slack in the congested parts. Referring more particularly to FIG. **2**, the steps involved in this process are, in general, as follows:

Initial placement of cells into bins (Step 1).

Calculation of delay estimates, i.e., slack estimates, and congestion estimates (Step 2).

Identification of critical paths and/or congested circuits (Step 3). In the case of congested circuits, identification of cells to be modified for in order for placement moves to relieve congestion.

Modification of logic to improve delay (Step 4), e.g., speeding up part of the circuit to improve slack in that part of the circuit. Conventional logic optimization techniques such as remapping and buffering are used for this. The purpose of this step is twofold. Such timing improvement is desirable in and of itself Also, if positive slack is achieved for parts of the congested circuit, this positive slack provides room for a subsequent placement step to move the cells in this part further away to reduce congestion.

Modification of logic to potentially improve circuit congestion (Step 5). Techniques such as fanout splitting are used for this.

Placement modification to take advantage of the preceding modifications (Step 6).

Undo logic modifications not used in the preceding placement modifications (Step 7).

Update slack and congestion estimates (Step 8).

Repeat for so long as significant improvement is obtained (Step 9).

Note that in various embodiments of the invention, not all of the foregoing steps may be practiced and that the order of the steps practiced may vary from the order of steps as presented above.

Particular logic modifications used to relieve congestion will be described in greater detail. Placement algorithms are limited in how they can place cells by the topology of the circuit. If the output of cell A is connected to (also referred to as "fanning out to") four different terminals in different cells (indicated by the numbers **1**–**4**) in FIG. **3**(*a*), then the placement of A is strongly influenced by the placement of cells corresponding to these terminals. In addition, because the output of A needs to be routed to four different places, the output of A is likely to cause congestion in this part of the circuit. Modifying the circuit topology without changing the logic functionality can avoid the bunching of wires at the output of A. This general step is referred to as fanout splitting. There are two distinct ways in which fanout splitting is done.

The first method involves buffering and is illustrated in FIG. **3**(*b*). Here buffers B and C are added such that B is used to drive terminals **1** and **2** and C is used to drive **3** and **4**. The grouping of terminals and assignments to buffers is done using geometric proximity of the terminals. Once the fanouts have been distributed between the buffers, a subsequent placement step can now move the buffers closer to the terminal they are connected to, relieving congestion due to the large fanout at the output of A.

In FIG. **3**(*c*) an alternative technique is used. Two copies of node A are used, labeled A1 and A2, with A1 fanning out to 1 and 2, and A2 fanning out to 3 and 4. This technique is referred to as node splitting. Once node splitting is done a subsequent placement step can move A1 or A2 closer to the terminals they are connected to, in order to relieve congestion.

To summarize, the steps involved in fanout splitting are:

Identification of congested bins. This is done using the congestion estimates for each bin.

Identification of large fanout cells resulting in congestion.

Modification of the circuit topology using fanout splitting by either buffering or node splitting.

Further examples of logic modifications that may be used to relieve congestion will now be described.

One measure of the congestion in a bin is given by pin density, calculated as the total number of pins in the bin divided by the total routable area in the bin. Here a pin refers to either an input or an output of a cell. It is desirable to get a lower congestion since that is likely to make routing easier. It is possible for logic optimizations to directly reduce this measure of congestion.

Intra-bin pin density logic optimization is done by replacing a set of gates in a bin with a different but logically equivalent set. Referring to FIG. 4(*a*), the AND gate followed by the NOR gate is logically equivalent to the AND-OR-INVERT gate shown in FIG. 4(*b*). In this case assume that the total routable area is the same before and after the logic change. However, the AND-OR-INVERT gate in FIG. 4(*b*) has fewer pins (4) compared to the AND and the NOR gates (3 each for a total of 6 pins) in FIG. 4(*a*). Intuitively, elimination of the extra net between the AND and the NOR gate in FIG. 4(*a*) will make the bin less congested.

Pin density can be reduced in a congested bin by possibly increasing it in a less congested bin. This technique is referred to as inter-bin logic optimization. FIG. 5(*a*) shows two AND gates in different bins. Assume that Bin 1 is over congested and Bin 2 is undercongested. By using the associative property of AND gates, a connection (C) can be moved from the AND gate in Bin 1 to that in Bin 2 as shown in FIG. 5(*b*). This reduces the pin density in Bin 1 (the number of pins is reduced from 4 to 3) and thus reduces congestion. Note that the pin density and thus the congestion in Bin 2 has increased in the process (the number of pins increases from 3 to 4), but that is acceptable since Bin 2 was undercongested.

Another logic optimization technique is input splitting. The motivation for this technique is similar to that for fanout splitting. A gate with a large number of input pins is replaced by a set of gates each one of which has a smaller number of input pins. While this may increase the pin density, it provides flexibility for a subsequent placement step to move some of these gates from an over congested bin to an undercongested bin in order to improve congestion.

FIG. 4(*b*) shows an AND-OR-INVERT gate with three inputs. Input splitting results in this gate being replaced by the an AND gate followed by a NOR gate as in FIG. 4(*a*). While this may result in increasing the pin density in the bin, it allows a subsequent placement step to move either of the two gates into a different undercongested bin.

FIG. 6(*a*) shows a three input AND gate. Input splitting results in this being replaced by two, two input AND gates as shown in FIG. 6(*b*). A subsequent placement step may now move either of these gates to a different undercongested bin.

For many of the congestion relieving logic synthesis methods proposed as part of placement, there are two important issues that this invention addresses. In most cases, logic synthesis cannot itself improve congestion, but rather only provide opportunities for placement to improve congestion, it is important to track which of these opportunities are actually used. Any unused opportunities may result in wasted resources, since the logic optimization step used to create them typically uses additional area and power (for faster cells) or additional gates. The use of the logic optimizations during placement is therefore actively tracked. Any unused optimizations are undone to ensure that there are no wasted resources.

It is important that the area used by the logic optimizations be monitored. Because the current placement (at the time of the logic optimizations) is based on a certain area of all the bins, if this information changes, then the placement may no longer be appropriate. The change may result in placement being done again at that step, and possibly the process never converging. Monitoring of the area used in order to preserve the feasibility of the placement is done by placing an upper bound on the area of each bin. The proposed logic optimizations are only allowed to increase the bin area to the upper bound. Bounding the increase in bin area guarantees convergence of the placement process.

The present invention may be embodied in various forms, including computer-implemented methods, computer systems configured to implement such methods, computer-readable media containing instructions for implementing such methods, etc. Examples of computer-implemented methods embodying the invention have been described. Reducing such methods to tangible form as computerreadable media may be accomplished by methods well-known in the art.

Referring to FIG. 7, a diagram is shown of a computer system that may be used to practice the present invention. Attached to a system bus are one or more CPUs, read-only memory (ROM), read/write memory (RAM), mass storage, and other I/O devices. The other I/O devices will typically include a keyboard, a pointing device, and a display, and may further include any of a wide variety of commercially-available I/O devices, including, for example, magnetic storage devices, optical storage devices, other storage devices, printers, etc. Stored within memory (e.g., RAM) is software (e.g., EDA software) implementing methods of the type previously described.

New deep submicron technologies are resulting in a much stronger dependence between the steps of logic optimization, cell placement and interconnection routing. Consequently, current design methodologies that handle these steps separately result in too many iterations over these steps and possibly no convergence, causing long delays in the design process. This invention will significantly reduce, if not eliminate, the iterations needed by considering not only the impact of interconnect during logic optimization of area/timing, but also at the same time doing logic optimization to help placement relieve congestion and thus generate a circuit that is easily routable.

It will be appreciated by those of ordinary skill in the art that the invention can be embodied in other specific forms without departing from the spirit or essential character thereof The presently disclosed embodiments are therefore considered in all respects to be illustrative and not restrictive. The scope of the invention is indicated by the appended claims rather than the foregoing description, and all changes which come within the meaning and range of equivalents thereof are intended to be embraced therein.

What is claimed is:

1. A method of modifying an integrated circuit design to facilitate placement of circuit elements within one or more regions called bins on an integrated circuit design layout, comprising the steps of:

performing an initial placement of integrated circuit elements within bins on the design layout;

calculating congestion of the initial placement; and

subject to limits on the increase in area of integrated circuit elements within a bin, performing logic modifications within selected bins of the integrated circuit design to allow congestion of the placement to be improved.

2. The method of claim 1, comprising the further step of performing placement refinement in an attempt to improve congestion by taking advantage of the logic modifications.

3. The method of claim 2, comprising the further steps of:

tracking logic modifications to determine which logic modifications resulted in placement modifications during placement refinement; and

undoing logic modifications that did not result in placement modifications.

4. The method of claim 2, comprising the further step of modifying logic within the integrated circuit design to improve timing performance of the integrated circuit design subject to limits on the increase in area of integrated circuit elements within a bin.

5. The method of claim 4, wherein modifying logic to improve timing performance comprises speeding up part of the circuit to improve timing slack in that part of the circuit.

6. The method of claim 2, comprising the further steps of:

calculating congestion of the placement following placement refinement; and

depending on the degree to which congestion has been improved, repeating said steps of modifying logic and performing placement refinement.

7. The method of claim 2, wherein modifying logic comprises replacing an original set of gates in the circuit with a different set of gates that is logically equivalent to the original set of gates.

8. The method of claim 7, wherein the different set of gates results in a lower ratio of number of pins to routable area in at least one bin.

9. The method of claim 7, wherein modifying logic comprises replacing a single gate having a plural number N of fanouts with a plurality of gates each having fewer than N fanouts.

10. The method of claim 7, wherein modifying logic comprises inserting buffers within a fanout tree of a gate.

11. The method of claim 7, wherein modifying logic comprises replacing a single gate having a plural number N of fanins with a plurality of gates each having fewer than N fanins.

12. A method of modifying an integrated circuit design to facilitate placement of circuit elements within one or more regions called bins on an integrated circuit design layout, comprising the steps of:

performing an initial placement of integrated circuit elements within bins on the design layout, connections between the integrated circuit elements being represented as nets within a netlist describing the integrated circuit design;

calculating congestion of the initial placement; and

subject to limits on the increase in area of integrated circuit elements within a bin, performing logic modifications within selected bins of the integrated circuit design;

wherein the logic modifications improve timing of selected nets belonging to the selected bins, reducing constraints on a subsequent placement step.

13. The method of claim 12, comprising the further step of performing placement refinement in an attempt to improve congestion by taking advantage of the logic modifications.

14. The method of claim 13, comprising the further steps of:

tracking logic modifications to determine which logic modifications resulted in placement modifications during placement refinement; and

undoing logic modifications that did not result in placement modifications.

15. A computer-readable medium including instructions for modifying an integrated circuit design to facilitate placement of circuit elements within one or more regions called bins on an integrated circuit design layout, including instructions for:

performing an initial placement of integrated circuit elements within bins on the design layout;

calculating congestion of the initial placement; and

subject to limits on the increase in area of integrated circuit elements within a bin, performing logic modifications within selected bins of the integrated circuit design to allow congestion of the placement to be improved.

16. A computer-readable medium including instructions for modifying an integrated circuit design to facilitate placement of circuit elements within one or more regions called bins on an integrated circuit design layout, including instructions for:

performing an initial placement of integrated circuit elements within bins on the design layout, connections between the integrated circuit elements being represented as nets within a netlist describing the integrated circuit design;

calculating congestion of the initial placement; and

subject to limits on the increase in area of integrated circuit elements within a bin, performing logic modifications within selected bins of the integrated circuit design;

wherein the logic modifications improve timing of selected nets belonging to the selected bins, reducing constraints on a subsequent placement step.

17. Apparatus for modifying an integrated circuit design to facilitate placement of circuit elements within one or more regions called bins on an integrated circuit design layout, comprising:

means for performing an initial placement of integrated circuit elements within bins on the design layout;

means for calculating congestion of the initial placement; and

means for, subject to limits on the increase in area of integrated circuit elements within a bin, performing logic modifications within selected bins of the integrated circuit design to allow congestion of the placement to be improved.

18. Apparatus for modifying an integrated circuit design to facilitate placement of circuit elements within one or more regions called bins on an integrated circuit design layout, comprising:

means for performing an initial placement of integrated circuit elements within bins on the design layout, connections between the integrated circuit elements being represented as nets within a netlist describing the integrated circuit design;

means for calculating congestion of the initial placement; and

means, subject to limits on the increase in area of integrated circuit elements within a bin, performing logic modifications within selected bins of the integrated circuit design;

wherein the logic modifications improve timing of selected nets belonging to the selected bins, reducing constraints on a subsequent placement step.

* * * * *

PATENT APPLICATION SERIAL NO. 09/097,816

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

PTO-1556
(5/87)

ABSTRACT OF THE DISCLOSURE

This invention recognizes the ability of logic optimization to help placement relieve congestion. Different types of logic optimizations are used to help placement relieve congestion. In one type of optimization, the speed of parts of the circuit is improved by selecting faster cells. In another type of optimization, the topology of the circuit is changed such that placement can now move cells, which could not have been moved before, to reduce congestion and thus enable routing. A distinguishing feature of this methodology is that it not only uses the placement information for interconnection delay/area estimates during logic optimization, but also uses logic optimization to aid the physical placement steps by providing support to placement so that the congestion of the circuit is improved. The aim is to avoid getting into a situation where the placed circuit cannot be routed.

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A METHOD FOR LOGIC OPTIMIZATION FOR IMPROVING TIMING AND CONGESTION DURING PLACEMENT IN INTEGRATED CIRCUIT DESIGN

This application is related by subject matter to U.S. Application Serial No. 09/097,317 (~~Atty. Dkt. No. M-5662-US~~) entitled METHOD FOR DESIGN OPTIMIZATION USING LOGICAL AND PHYSICAL INFORMATION, filed on even date herewith and incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to integrated circuit design and layout.

2. State of the Art

Traditional cell-based integrated circuit design follows several steps. The first step is designing the logical gate-level circuit that implements the function to be realized by the circuit (referred to as logic design or logic synthesis, of which logic optimizations are a key part). The next step is placing the gates (or cells) in a physical layout, and the final step is routing the interconnection between the cells. With increasing dominance of interconnection delays and area in circuits implemented in deep submicron technologies, this approach is proving to be no longer viable. The problem is that, during the logic optimization stage, the interconnection is not known yet, and thus the dominant part of the area and the delay cannot be considered.

Attempts to overcome this problem have considered alternating logic synthesis and placement and routing, with "back annotation" of the interconnect information to the subsequent logic synthesis steps. Referring to Figure 1, showing traditional cell-based design flow, a logic design phase is followed by a cell placement phase and then a routing phase. Following the routing phase, interconnection data is back annotated. The logic design, cell placement and routing phases are then repeated. This cycle is continued until, during the routing phase, the design is

successfully routed. The problem with this method is that the logic synthesis steps that consider the back annotation information cannot guarantee to fix problems that prevent routing without introducing additional problems due to the modifications made to the circuit gates and topology. There results a large number of iterations between logic synthesis and subsequent place and route, with the possibility of the process never converging.

An alternative approach is to consider placement information during logic optimization. In this methodology, sometimes termed "placement aware synthesis," placement information is made available in varying degrees during logic optimization, i.e. some placement is done as part of logic synthesis (sometimes referred to in the industry as just synthesis). Logic optimization uses this placement information to estimate the effect of the interconnects on the delay and the area of the circuit. Thus logic optimization attempts to accurately model the interconnect delay and area that might result during a placement step. However, it may result in a placed circuit that cannot be routed using the area resources provided by the placement step. The inability to route the resulting placed circuit results in modifications to the placement, consequently nullifying the interconnection information used during logic optimization.

A circuit that has been placed but cannot be routed subject to the available area constraints is not realizable. Additional routing resources must be created to enable the routing. There results an increase in circuit area and possibly delay, since the wires may now need to go through longer paths.

Placement algorithms are limited in how they can place cells by the timing constraints placed on the design. The timing constraints may result in certain parts of the design being very congested in terms of the wiring (or interconnection) resources needed to connect the cells in those parts of the circuit. It would be possible to relieve the congestion if somehow the cells in the congested area were to be moved apart. However, moving the cells apart may result in an increase in the

interconnection delays, which in turn may result in a violation of the timing constraints. Thus a situation results where it is possible to have acceptable timing slacks or acceptable congestion but not both.

The paper by Villarubia and Hojat (ICCD 97) proposes integrated logic optimization and placement. However, the proposed methodology alternates placement and logic optimization and does not consider the impact of the logic optimizations on subsequent placement steps.

SUMMARY OF THE INVENTION

This invention recognizes the ability of logic optimization to help placement relieve congestion. Different types of logic optimizations are used to help placement relieve congestion. In one type of optimization, the speed of parts of the circuit is improved by selecting faster cells. In another type of optimization, the topology of the circuit is changed such that placement can now move cells, which could not have been moved before, to reduce congestion and thus enable routing. A distinguishing feature of this methodology is that it not only uses the placement information for interconnection delay/area estimates during logic optimization, but also uses logic optimization to aid the physical placement steps by providing support to placement so that the congestion of the circuit is improved. The aim is to avoid getting into a situation where the placed circuit cannot be routed.

There are two specific ways in which logic optimization aids placement in relieving congestion. The first method involves determining parts of the circuit which are congested, and then speeding up the logic in these parts. This speedup provides timing slack for a subsequent placement step to move cells while ensuring that this move does not cause the modified interconnections to violate timing constraints. The second method involves modifying the topology of the circuit by adding gates while maintaining the functionality, such that the added gates can then be moved by the placement steps to relieve congestion.

An important aspect of the optimizations, specifically directed towards

helping placement relieve congestion, is the ability to undo modifications if placement does not actually use the modifications. The undo capability ensures that no area/power resources are wasted for transformations that are not used as intended.

A critical problem in using logic optimization as part of placement is that logic optimization steps can and do increase the area of circuits. This increase in area can invalidate the results of any placement done thus far, and consequently result in the inability of the combination of these steps to converge. An important part of this invention is to actively bound the area increase of specific parts of the circuit which guarantees that the current placement results are still valid after the logic optimizations, consequently guaranteeing convergence of the integrated logic optimization and placement steps.

BRIEF DESCRIPTION OF THE DRAWING

The present invention may be further understood from the following description in conjunction with the appended drawing. In the drawing:

Figure 1 is a flowchart of traditional cell-based design flow;

Figure 2 is a flowchart of design flow in accordance with the present invention;

Figure 3(a) is a diagram of a gate having a large fanout;

Figure 3(b) is a diagram of the gate of Figure 3(a) following fanout splitting using buffering;

Figure 3(c) is a diagram of a circuit equivalent to the gate of Figure 3(a) following fanout splitting using node splitting;

Figure 4(a) is a diagram of a circuit to which intra-bin pin density logic optimization may be applied;

Figure 4(b) is a diagram of an equivalent circuit resulting from intra-bin pin density logic optimization applied to the circuit of Figure 4(a);

Figure 5(a) is a diagram of a circuit to which inter-bin pin density logic optimization may be applied;

Figure 5(b) is a diagram of an equivalent circuit resulting from inter-bin pin density logic optimization applied to the circuit of Figure 5(a);

Figure 6(a) is a diagram of a circuit to which input splitting logic optimization may be applied;

Figure 6(b) is a diagram of an equivalent circuit resulting from input splitting logic optimization applied to the circuit of Figure 6(a);

Figure 7 is a block diagram of a computer system that may be used to practice the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention may be used in conjunction with an electronic design automation placement tool. In accordance with an exemplary embodiment of one such placement tool, at each stage in cell placement, the cells are partitioned into a number of bins. Interconnection models for interconnects between bins and within bins provide both delay estimates for each interconnect in the circuit, as well as congestion estimates for each bin in the circuit. The circuit has timing constraints imposed on it that it needs to satisfy. The delay estimates of the interconnection, combined with the delays of the cells and the timing constraints imposed on the design, are converted to timing slack information for each part of the circuit. A negative timing slack indicates that that part of the circuit is not meeting the timing constraints. A positive slack indicates that that part of the circuit is producing its result faster than is needed and can thus be slowed down without violating its timing constraints. More generally, "slack" is defined herein as a measure of the degree to which a timing requirement is met in an integrated circuit design.

The traditional role of logic synthesis has been to identify areas of the circuit which have negative timing slack and then modify the circuit so as to fix this problem. As described herein, logic synthesis is used to aid placement to achieve both acceptable delays and congestion, by making circuit modifications that increase the timing slack in the congested parts. Referring more particularly to Figure 2, the steps involved in this process are, in general, as follows:

- Initial placement of cells into bins (Step 1).

- Calculation of delay estimates, i.e., slack estimates, and congestion estimates (Step 2).
- Identification of critical paths and/or congested circuits (Step 3). In the case of congested circuits, identification of cells to be modified for in order for placement moves to relieve congestion.
- Modification of logic to improve delay (Step 4), e.g., speeding up part of the circuit to improve slack in that part of the circuit. Conventional logic optimization techniques such as remapping and buffering are used for this. The purpose of this step is twofold. Such timing improvement is desirable in and of itself. Also, if positive slack is achieved for parts of the congested circuit, this positive slack provides room for a subsequent placement step to move the cells in this part further away to reduce congestion.
- Modification of logic to potentially improve circuit congestion (Step 5). Techniques such as fanout splitting are used for this.
- Placement modification to take advantage of the preceding modifications (Step 6).
- Undo logic modifications not used in the preceding placement modifications (Step 7).
- Update slack and congestion estimates (Step 8).
- Repeat for so long as significant improvement is obtained (Step 9).

Note that in various embodiments of the invention, not all of the foregoing steps may be practiced and that the order of the steps practiced may vary from the order of steps as presented above.

Particular logic modifications used to relieve congestion will be described in greater detail. Placement algorithms are limited in how they can place cells by the topology of the circuit. If the output of cell A is connected to (also referred to as "fanning out to") four different terminals in different cells (indicated by the numbers 1-4) in Figure 3(a), then the placement of A is strongly influenced by the placement of cells corresponding to these terminals. In addition, because the output of A needs to be routed to four different places, the output of A is likely to cause congestion in this part of the circuit. Modifying the circuit topology without changing the logic functionality can avoid the bunching of wires at the output of A. This general step is referred to as fanout splitting. There are two distinct ways in which fanout splitting is done.

The first method involves buffering and is illustrated in Figure 3(b). Here

buffers B and C are added such that B is used to drive terminals 1 and 2 and C is used to drive 3 and 4. The grouping of terminals and assignments to buffers is done using geometric proximity of the terminals. Once the fanouts have been distributed between the buffers, a subsequent placement step can now move the buffers closer to the terminal they are connected to, relieving congestion due to the large fanout at the output of A.

In Figure 3(c) an alternative technique is used. Two copies of node A are used, labeled A1 and A2, with A1 fanning out to 1 and 2, and A2 fanning out to 3 and 4. This technique is referred to as node splitting. Once node splitting is done a subsequent placement step can move A1 or A2 closer to the terminals they are connected to, in order to relieve congestion.

To summarize, the steps involved in fanout splitting are:

- Identification of congested bins. This is done using the congestion estimates for each bin.
- Identification of large fanout cells resulting in congestion.
- Modification of the circuit topology using fanout splitting by either buffering or node splitting.

Further examples of logic modifications that may be used to relieve congestion will now be described.

One measure of the congestion in a bin is given by pin density, calculated as the total number of pins in the bin divided by the total routable area in the bin. Here a pin refers to either an input or an output of a cell. It is desirable to get a lower congestion since that is likely to make routing easier. It is possible for logic optimizations to directly reduce this measure of congestion.

Intra-bin pin density logic optimization is done by replacing a set of gates in a bin with a different but logically equivalent set. Referring to Figure 4(a), the AND gate followed by the NOR gate is logically equivalent to the AND-OR-INVERT gate shown in Figure 4(b). In this case assume that the total routable area is the same before and after the logic change. However, the AND-OR-INVERT

gate in Figure 4(b) has fewer pins (4) compared to the AND and the NOR gates (3 each for a total of 6 pins) in Figure 4(a). Intuitively, elimination of the extra net between the AND and the NOR gate in Figure 4(a) will make the bin less congested.

Pin density can be reduced in a congested bin by possibly increasing it in a less congested bin. This technique is referred to as inter-bin logic optimization. Figure 5(a) shows two AND gates in different bins. Assume that Bin 1 is over congested and Bin 2 is undercongested. By using the associative property of AND gates, a connection (C) can be moved from the AND gate in Bin 1 to that in Bin 2 as shown in Figure 5(b). This reduces the pin density in Bin 1 (the number of pins is reduced from 4 to 3) and thus reduces congestion. Note that the pin density and thus the congestion in Bin 2 has increased in the process (the number of pins increases from 3 to 4), but that is acceptable since Bin 2 was undercongested.

Another logic optimization technique is input splitting. The motivation for this technique is similar to that for fanout splitting. A gate with a large number of input pins is replaced by a set of gates each one of which has a smaller number of input pins. While this may increase the pin density, it provides flexibility for a subsequent placement step to move some of these gates from an over congested bin to an undercongested bin in order to improve congestion.

Figure 4(b) shows an AND-OR-INVERT gate with three inputs. Input splitting results in this gate being replaced by the an AND gate followed by a NOR gate as in Figure 4(a). While this may result in increasing the pin density in the bin, it allows a subsequent placement step to move either of the two gates into a different undercongested bin.

Figure 6(a) shows a three input AND gate. Input splitting results in this being replaced by two, two input AND gates as shown in Figure 6(b). A subsequent placement step may now move either of these gates to a different undercongested bin.

For many of the congestion relieving logic synthesis methods proposed as part of placement, there are two important issues that this invention addresses. In most cases, logic synthesis cannot itself improve congestion, but rather only provide opportunities for placement to improve congestion, it is important to track which of these opportunities are actually used. Any unused opportunities may result in wasted resources, since the logic optimization step used to create them typically uses additional area and power (for faster cells) or additional gates. The use of the logic optimizations during placement is therefore actively tracked. Any unused optimizations are undone to ensure that there are no wasted resources.

It is important that the area used by the logic optimizations be monitored. Because the current placement (at the time of the logic optimizations) is based on a certain area of all the bins, if this information changes, then the placement may no longer be appropriate. The change may result in placement being done again at that step, and possibly the process never converging. Monitoring of the area used in order to preserve the feasibility of the placement is done by placing an upper bound on the area of each bin. The proposed logic optimizations are only allowed to increase the bin area to the upper bound. Bounding the increase in bin area guarantees convergence of the placement process.

The present invention may be embodied in various forms, including computer-implemented methods, computer systems configured to implement such methods, computer-readable media containing instructions for implementing such methods, etc. Examples of computer-implemented methods embodying the invention have been described. Reducing such methods to tangible form as computer-readable media may be accomplished by methods well-known in the art.

Referring to Figure 7, a diagram is shown of a computer system that may be used to practice the present invention. Attached to a system bus are one or more CPUs, read-only memory (ROM), read/write memory (RAM), mass storage, and other I/O devices. The other I/O devices will typically include a keyboard, a point-

ing device, and a display, and may further include any of a wide variety of commercially-available I/O devices, including, for example, magnetic storage devices, optical storage devices, other storage devices, printers, etc. Stored within memory (e.g., RAM) is software (e.g., EDA software) implementing methods of the type previously described.

New deep submicron technologies are resulting in a much stronger dependence between the steps of logic optimization, cell placement and interconnection routing. Consequently, current design methodologies that handle these steps separately result in too many iterations over these steps and possibly no convergence, causing long delays in the design process. This invention will significantly reduce, if not eliminate, the iterations needed by considering not only the impact of interconnect during logic optimization of area/timing, but also at the same time doing logic optimization to help placement relieve congestion and thus generate a circuit that is easily routable.

It will be appreciated by those of ordinary skill in the art that the invention can be embodied in other specific forms without departing from the spirit or essential character thereof. The presently disclosed embodiments are therefore considered in all respects to be illustrative and not restrictive. The scope of the invention is indicated by the appended claims rather than the foregoing description, and all changes which come within the meaning and range of equivalents thereof are intended to be embraced therein.

What is claimed is:

1. A method of modifying an integrated circuit design to facilitate placement of circuit elements on an integrated circuit design layout, comprising the steps of:

performing an initial placement of integrated circuit elements within bins on the design layout;

calculating congestion of the initial placement; and

subject to limits on the increase in area of integrated circuit elements within a bin, performing logic modifications within selected bins of the integrated circuit design to allow congestion of the placement to be improved.

2. The method of Claim 1, comprising the further step of performing placement refinement in an attempt to improve congestion by taking advantage of the logic modifications.

3. The method of Claim 2, comprising the further steps of:

tracking logic modifications to determine which logic modifications resulted in placement modifications during placement refinement; and

undoing logic modifications that did not result in placement modifications.

4. The method of Claim 2, comprising the further step of modifying logic within the integrated circuit design to improve timing performance of the integrated circuit design subject to limits on the increase in area of integrated circuit elements within a bin.

5. The method of Claim 4, wherein modifying logic to improve timing performance comprises speeding up part of the circuit to improve timing slack in that part of the circuit.

6. The method of Claim 2, comprising the further steps of:

calculating congestion of the placement following placement refinement; and

depending on the degree to which congestion has been improved, repeating said steps of modifying logic and performing placement refinement.

7. The method of Claim 2, wherein modifying logic comprises replacing an original set of gates in the circuit with a different set of gates that is logically equivalent to the original set of gates.

8. The method of Claim 7, wherein the different set of gates results in a lower ratio of number of pins to routable area in at least one bin.

9. The method of Claim 7, wherein modifying logic comprises replacing a single gate having a plural number N of fanouts with a plurality of gates each having fewer than N fanouts.

10. The method of Claim 7, wherein modifying logic comprises inserting buffers within a fanout tree of a gate.

11. The method of Claim 7, wherein modifying logic comprises replacing a single gate having a plural number N of fanins with a plurality of gates each having fewer than N fanins.

12. A method of modifying an integrated circuit design to facilitate placement of circuit elements on an integrated circuit design layout, comprising the steps of:

performing an initial placement of integrated circuit elements within bins on the design layout, connections between the integrated circuit elements being represented as nets within a netlist describing the integrated circuit design;

calculating congestion of the initial placement; and

subject to limits on the increase in area of integrated circuit elements within a bin, performing logic modifications within selected bins of the integrated circuit design;

wherein the logic modifications improve timing of selected nets belonging to the selected bins, reducing constraints on a subsequent placement step.

13. The method of Claim 12, comprising the further step of performing placement refinement in an attempt to improve congestion by taking advantage of the logic modifications.

14. The method of Claim 13, comprising the further steps of:

tracking logic modifications to determine which logic modifications resulted in placement modifications during placement refinement; and

undoing logic modifications that did not result in placement modifications.

15. A computer-readable medium including instructions for modifying an integrated circuit design to facilitate placement of circuit elements on an integrated circuit design layout, including instructions for:

performing an initial placement of integrated circuit elements within bins on the design layout;

calculating congestion of the initial placement; and

subject to limits on the increase in area of integrated circuit elements within a bin, performing logic modifications within selected bins of the integrated circuit design to allow congestion of the placement to be improved.

16. A computer-readable medium including instructions for modifying an integrated circuit design to facilitate placement of circuit elements on an integrated circuit design layout, including instructions for:

performing an initial placement of integrated circuit elements within bins on the design layout, connections between the integrated circuit elements being represented as nets within a netlist describing the integrated circuit design;

calculating congestion of the initial placement; and

subject to limits on the increase in area of integrated circuit elements within a bin, performing logic modifications within selected bins of the integrated circuit design;

wherein the logic modifications improve timing of selected nets belonging to the selected bins, reducing constraints on a subsequent placement step.

17. Apparatus for modifying an integrated circuit design to facilitate placement of circuit elements on an integrated circuit design layout, comprising:

means for performing an initial placement of integrated circuit elements within bins on the design layout;

means for calculating congestion of the initial placement; and

means for, subject to limits on the increase in area of integrated cir-

cuit elements within a bin, performing logic modifications within selected bins of the integrated circuit design to allow congestion of the placement to be improved.

18. Apparatus for modifying an integrated circuit design to facilitate placement of circuit elements on an integrated circuit design layout, comprising:

means for performing an initial placement of integrated circuit elements within bins on the design layout, connections between the integrated circuit elements being represented as nets within a netlist describing the integrated circuit design;

means for calculating congestion of the initial placement; and

means, subject to limits on the increase in area of integrated circuit elements within a bin, performing logic modifications within selected bins of the integrated circuit design;

wherein the logic modifications improve timing of selected nets belonging to the selected bins, reducing constraints on a subsequent placement step.

COMBINED DECLARATION AND POWER OF ATTORNEY FOR UTILITY PATENT APPLICATION	Attorney's Docket No. 032260-004

As a below-named inventor, I hereby declare that:
My residence, post office address and citizenship are as stated below next to my name;
I BELIEVE I AM THE ORIGINAL, FIRST AND SOLE INVENTOR (if only one name is listed below) OR AN ORIGINAL, FIRST AND JOINT INVENTOR (if more than one name is listed below) OF THE SUBJECT MATTER WHICH IS CLAIMED AND FOR WHICH A PATENT IS SOUGHT ON THE INVENTION ENTITLED:

A METHOD FOR LOGIC OPTIMIZATION FOR IMPROVING TIMING AND CONGESTION DURING PLACEMENT IN INTEGRATED CIRCUIT DESIGN

the specification of which

(check one) ☒ is attached hereto;
☐ was filed on _____ as
Application No. _____
and was amended on _____; (if applicable)

I HAVE REVIEWED AND UNDERSTAND THE CONTENTS OF THE ABOVE-IDENTIFIED SPECIFICATION, INCLUDING THE CLAIMS, AS AMENDED BY ANY AMENDMENT REFERRED TO ABOVE;

I ACKNOWLEDGE THE DUTY TO DISCLOSE TO THE OFFICE ALL INFORMATION KNOWN TO ME TO BE MATERIAL TO PATENTABILITY AS DEFINED IN TITLE 37, CODE OF FEDERAL REGULATIONS, Sec. 1.56 (as amended effective March 16, 1992);

I do not know and do not believe the said invention was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to said application; that said invention was not in public use or on sale in the United States of America more than one year prior to said application; that said invention has not been patented or made the subject of an inventor's certificate issued before the date of said application in any country foreign to the United States of America on any application filed by me or my legal representatives or assigns more than twelve months prior to said application;

I hereby claim foreign priority benefits under Title 35, United States Code Sec. 119 and/or Sec. 365 of any foreign application(s) for patent or inventor's certificate as indicated below and have also identified below any foreign application for patent or inventor's certificate on this invention having a filing date before that of the application(s) on which priority is claimed:

COMBINED DECLARATION AND POWER OF ATTORNEY			Attorney's Docket No. 032260-004
COUNTRY/INTERNATIONAL	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED
			YES_ NO_
			YES_ NO_

I hereby appoint the following attorneys and agent(s) to prosecute said application and to transact all business in the Patent and Trademark Office connected therewith and to file, prosecute and to transact all business in connection with international applications directed to said invention:

William L. Mathis	17,337	Robert G. Mukai	28,531	Bruce J. Boggs, Jr.	32,344
Peter H. Smolka	15,913	George A. Hovanec, Jr.	28,223	William H. Benz	25,952
Robert S. Swecker	19,885	James A. LaBarre	28,632	Peter K. Skiff	31,917
Platon N. Mandros	22,124	E. Joseph Gess	28,510	Richard J. McGrath	29,195
Benton S. Duffett, Jr.	22,030	R. Danny Huntington	27,903	Matthew L. Schneider	32,814
Joseph R. Magnone	24,239	Eric H. Weisblatt	30,505	Michael G. Savage	32,596
Norman H. Stepno	22,716	James W. Peterson	26,057	Gerald F. Swiss	30,113
Ronald L. Grudziecki	24,970	Teresa Stanek Rea	30,427	Michael J. Ure	33,089
Frederick G. Michaud, Jr.	26,003	Robert E. Krebs	25,885	Charles F. Wieland III	33,096
Alan E. Kopecki	25,813	Robert M. Schulman	31,196	Bruce T. Wieder	33,815
Regis E. Slutter	26,999	William C. Rowland	30,888	Todd R. Walters	34,040
Samuel C. Miller, III	27,360	T. Gene Dillahunty	25,423		
Ralph L. Freeland, Jr.	16,110	Patrick C. Keane	32,858		

and: _____

Address all correspondence to: Robert E. Krebs
BURNS, DOANE, SWECKER & MATHIS, L.L.P.
P.O. Box 1404
Alexandria, Virginia 22313-1404

Address all telephone calls to: Michael J. Ure at (650) 854-7400.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

FULL NAME OF SOLE OR FIRST INVENTOR	SIGNATURE	DATE
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POST OFFICE ADDRESS		
40 Western Way, Princeton, NJ 08540, United States of America		
FULL NAME OF SECOND JOINT INVENTOR, IF ANY	SIGNATURE	DATE
Lawrence Pileggi		
RESIDENCE	CITIZENSHIP	
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POST OFFICE ADDRESS		
357 Dorseyville Road, Pittsburgh, PA 15215, United States of America		
FULL NAME OF THIRD JOINT INVENTOR, IF ANY	SIGNATURE	DATE
Abhijeet Chakraborty		
RESIDENCE	CITIZENSHIP	
710 Durshire Way, Sunnyvale, CA 94087, United States of America	India	
POST OFFICE ADDRESS		
710 Durshire Way, Sunnyvale, CA 94087, United States of America		

COMBINED DECLARATION AND POWER OF ATTORNEY		Attorney's Docket No. 032260-004
FULL NAME OF FOURTH JOINT INVENTOR, IF ANY Gary K. Yeap	SIGNATURE	DATE
RESIDENCE 3406 Grossmont Drive, San Jose, CA 95132, United States of America		CITIZENSHIP Malaysia
POST OFFICE ADDRESS 3406 Grossmont Drive, San Jose, CA 95132, United States of America		
FULL NAME OF FIFTH JOINT INVENTOR, IF ANY Douglas B. Boyle	SIGNATURE	DATE
RESIDENCE 385 Calcaterra Place, Palo Alto, CA 94306, United States of America		CITIZENSHIP United States of America
POST OFFICE ADDRESS 385 Calcaterra Place, Palo Alto, CA 94306, United States of America		

PRINT OF DRAWINGS
AS ORIGINALLY FILED

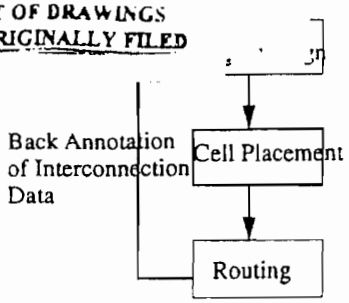


Fig 1

Traditional Cell Based Design Flow

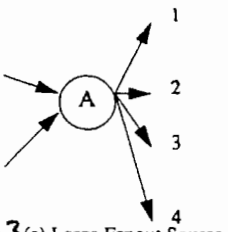


Fig 3(a) Large Fanout Source of Congestion

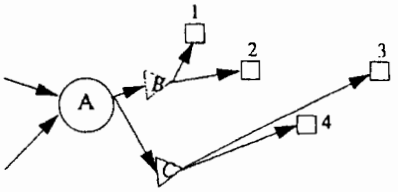


Fig 3(b) Fanout Splitting using Buffering

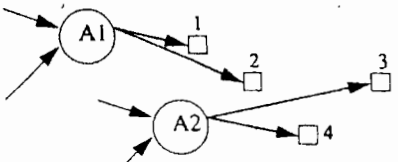


Fig 3(c) Fanout Splitting Using Node Splitting

PRINT OF DRAWINGS
AS ORIGINALLY FILED

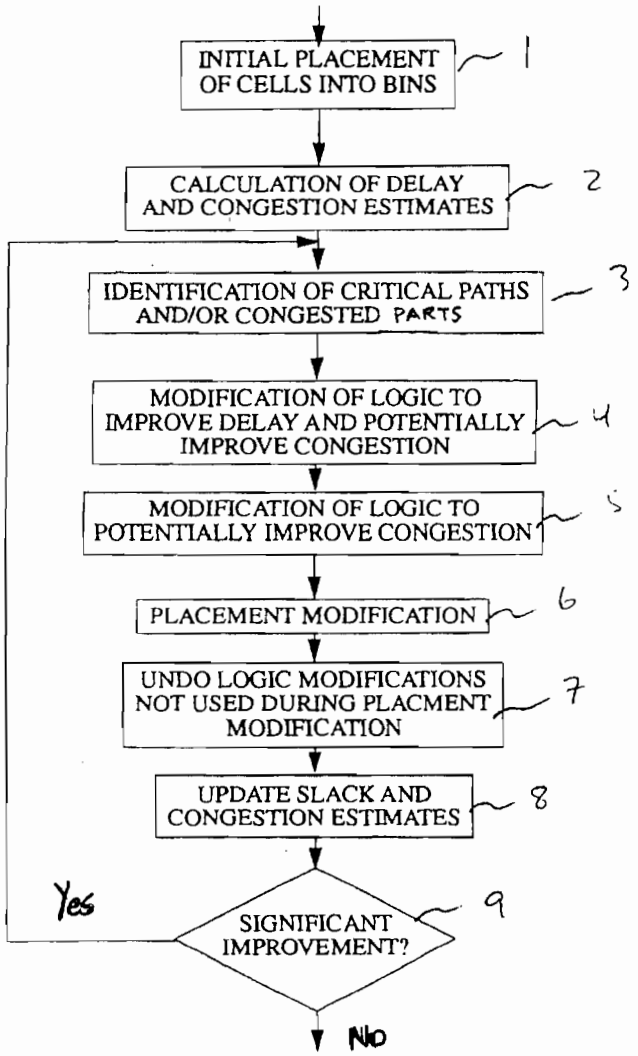
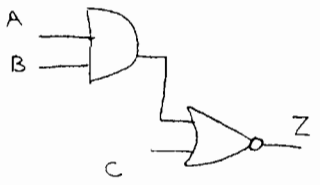


Fig 2

PRINT OF DRAWINGS
AS ORIGINALLY FILED



BOTH GATES ARE IN THE SAME BIN

Figure 4 (a)

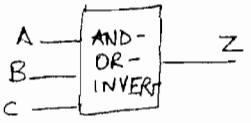


Figure 4(b)

DESIGNATED CONFIDENTIAL

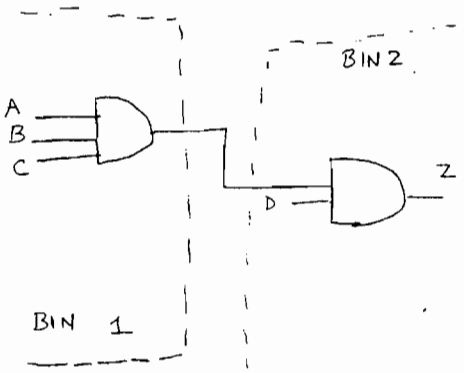


Figure 5 (a)

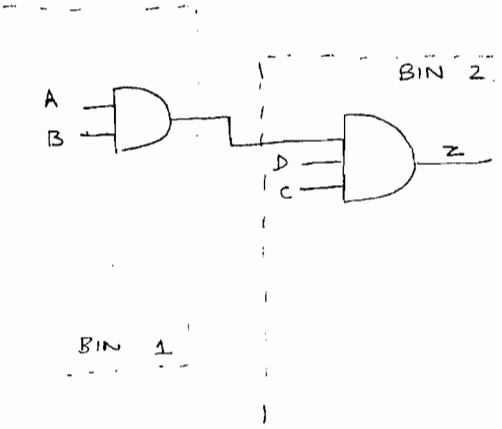


Figure 5 (b)

PRINT OF DRAWINGS
AS ORIGINALLY FILED

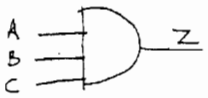


Figure 6(a)

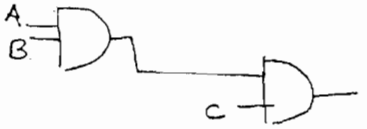


Figure 6(b).

EXHIBIT 5 PAGE 5 OF 5

PRINT OF DRAWINGS
AS ORIGINALLY FILED

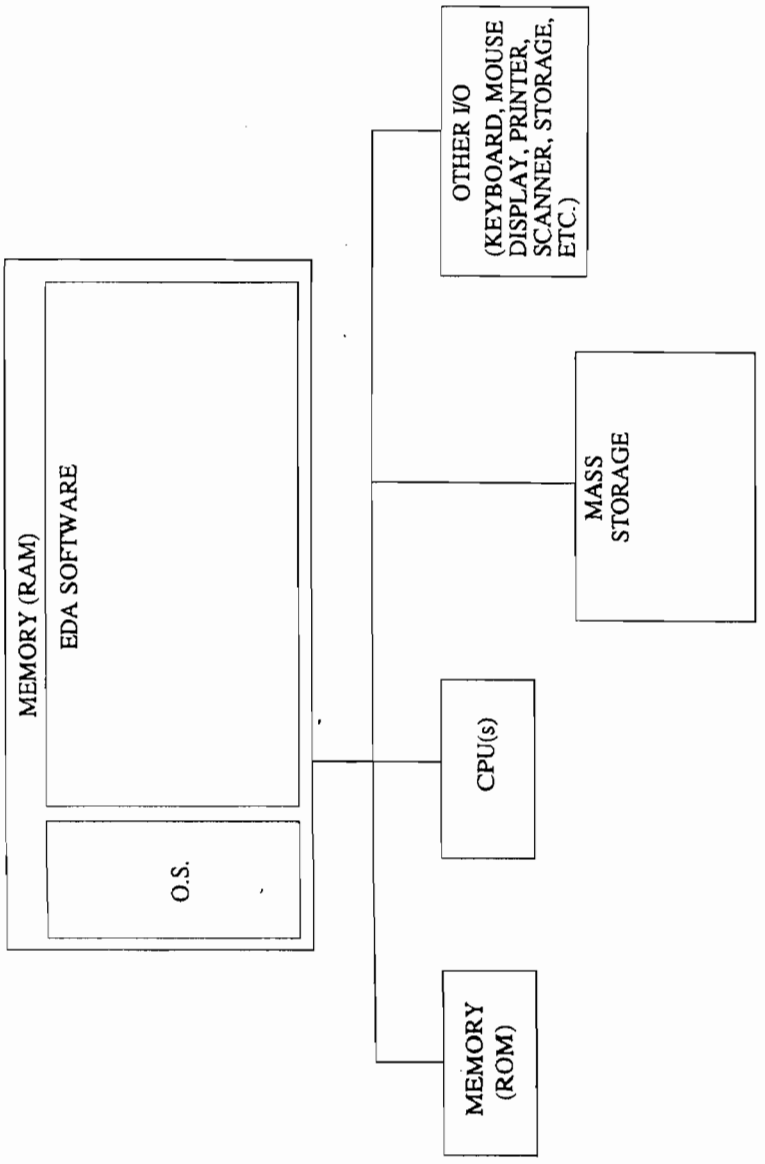


Fig. 7

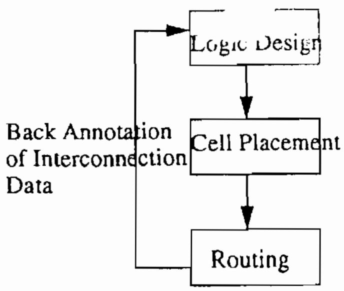


Fig 1

Traditional Cell Based Design Flow

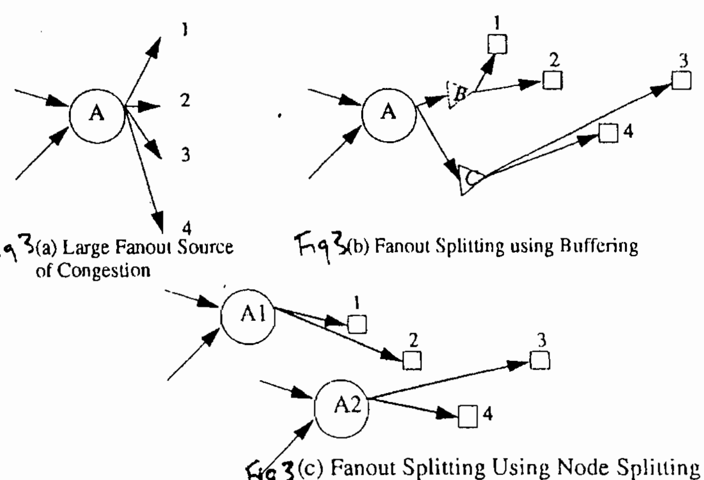


Fig 3(a) Large Fanout Source of Congestion

Fig 3(b) Fanout Splitting using Buffering

Fig 3(c) Fanout Splitting Using Node Splitting

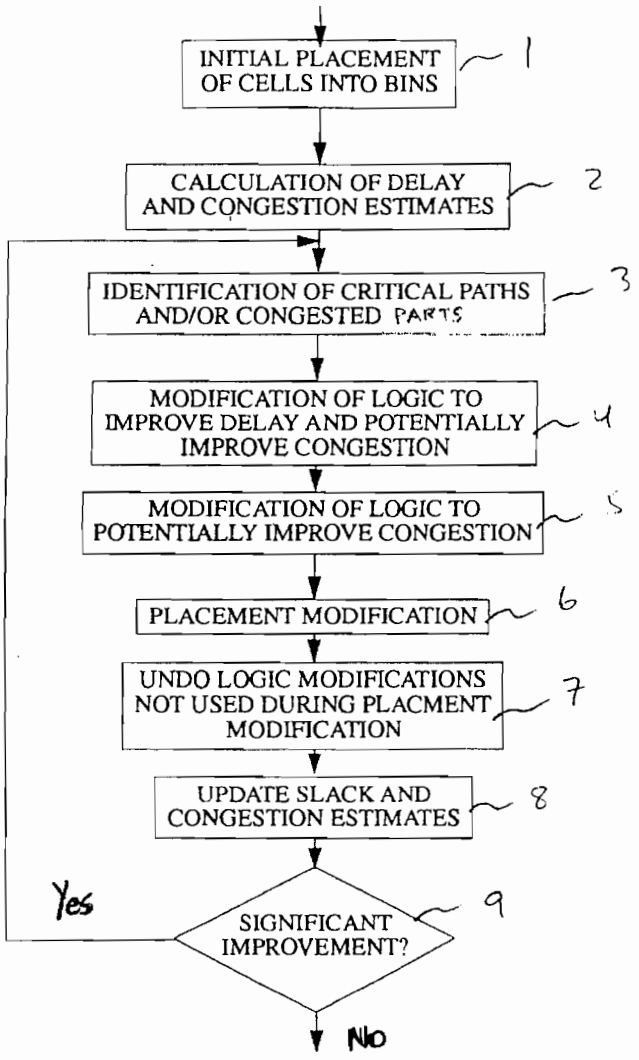

INITIAL PLACEMENT OF CELLS INTO BINS
1
CALCULATION OF DELAY AND CONGESTION ESTIMATES
2
IDENTIFICATION OF CRITICAL PATHS AND/OR CONGESTED PARTS
3
MODIFICATION OF LOGIC TO IMPROVE DELAY AND POTENTIALLY IMPROVE CONGESTION
4
MODIFICATION OF LOGIC TO POTENTIALLY IMPROVE CONGESTION
5
PLACEMENT MODIFICATION
6
UNDO LOGIC MODIFICATIONS NOT USED DURING PLACMENT MODIFICATION
7
UPDATE SLACK AND CONGESTION ESTIMATES
8
Yes
SIGNIFICANT IMPROVEMENT?
9
No

Fig 2

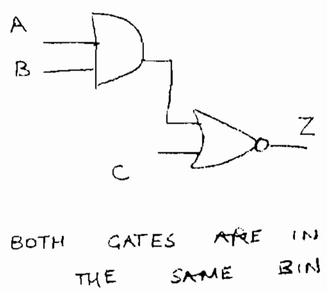


Figure 4 (a)

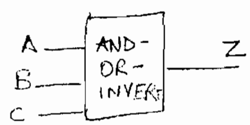


Figure 4(b)

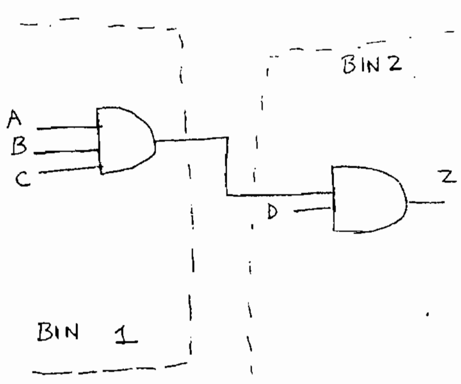


Figure 5 (a)

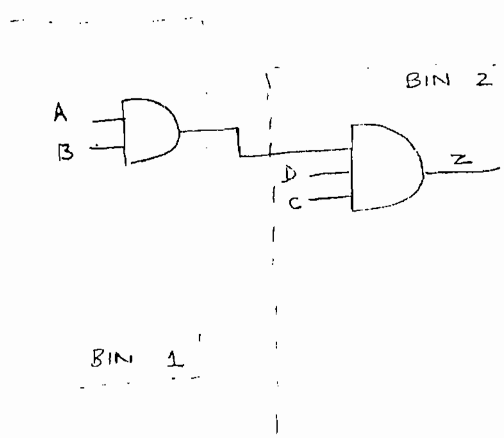


Figure 5 (b)

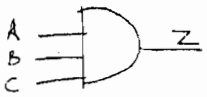


Figure 6(a)

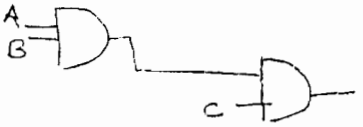


Figure 6(b).

SUBSTITUTE SHEET (RULE 26)

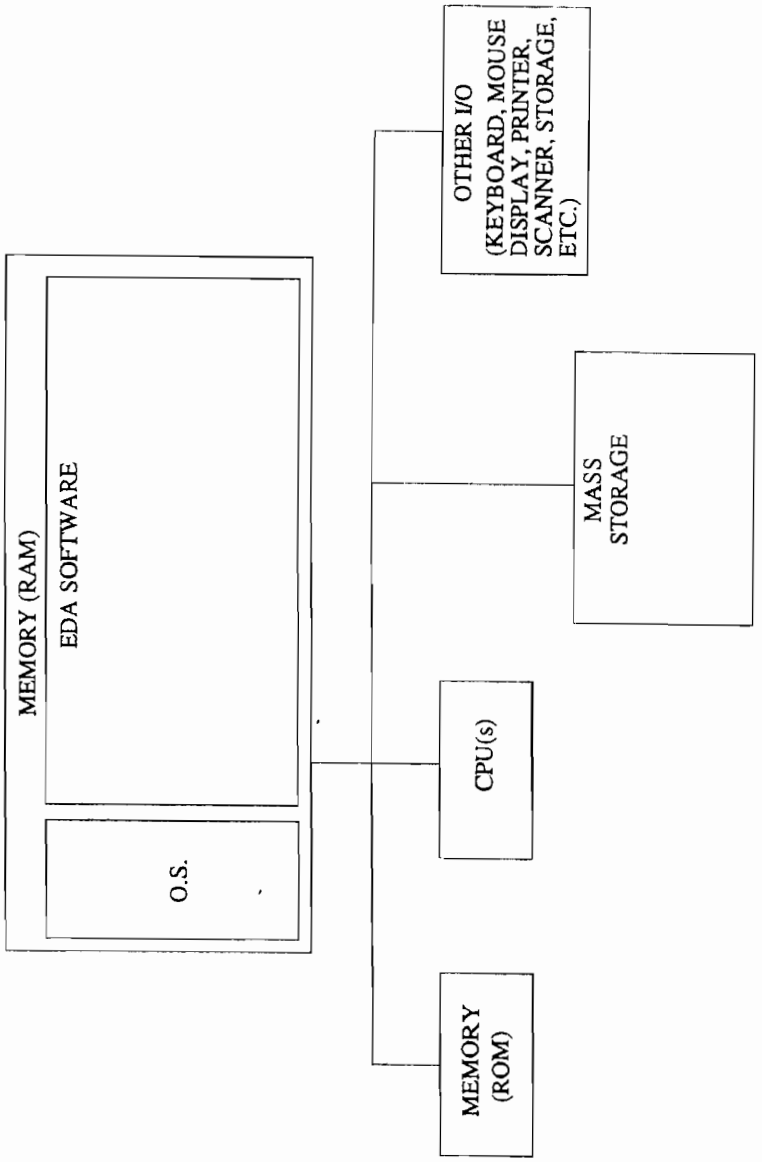

MEMORY (RAM)
EDA SOFTWARE
O.S.
CPU(s)
MEMORY (ROM)
MASS STORAGE
OTHER I/O (KEYBOARD, MOUSE DISPLAY, PRINTER, SCANNER, STORAGE, ETC.)

Fig. 7

PATENT APPLICATION FEE DETERMINATION RECORD

Effective October 1, 1997

Application or Docket Number: 09/097,076

CLAIMS AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA
BASIC FEE		
TOTAL CLAIMS	18 minus 20 =	*
INDEPENDENT CLAIMS	6 minus 3 =	* 3
MULTIPLE DEPENDENT CLAIM PRESENT	N	

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE [ ]	RATE	FEE	OR	OTHER THAN SMALL ENTITY	RATE	FEE
		395.00	OR			790.00
x$11=			OR	x$22=		
x41=			OR	x82=	3	246.00
+135=			OR	+270=	1	
TOTAL			OR	TOTAL		1036.00

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

SMALL ENTITY	RATE	ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY	RATE	ADDITIONAL FEE
x$11=			OR	x$22=		
x41=			OR	x82=		
+135=			OR	+270=		
TOTAL ADDIT. FEE			OR	TOTAL ADDIT. FEE		

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

RATE	ADDITIONAL FEE	OR	RATE	ADDITIONAL FEE
x$11=		OR	x$22=	
x41=		OR	x82=	
+135=		OR	+270=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

RATE	ADDITIONAL FEE	OR	RATE	ADDITIONAL FEE
x$11=		OR	x$22=	
x41=		OR	x82=	
+135=		OR	+270=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

FORM PTO-875 (Rev. 8/97) *U.S. Government Printing Office: 1997 - 430-571/69194 Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

SERIAL NUMBER	FILING DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
09/097,076	06/12/98	364	2763	032260-004

APPLICANT

SHARAD MALIK, PRINCETON, NJ; LAWRENCE PILEGGI, PITTSBURGH, PA; ABHIJEET CHAKRABORTY, SUNNYVALE, CA; GARY K. YEAP, SAN JOSE, CA; DOUGLAS B. BOYLE, PALO ALTO, CA.

CONTINUING DOMESTIC DATA********
VERIFIED

none

371 (NAT'L STAGE) DATA********
VERIFIED

none

FOREIGN APPLICATIONS********
VERIFIED

none

FOREIGN FILING LICENSE GRANTED 07/01/98 ***** SMALL ENTITY *****

Foreign Priority claimed 35 USC 119 (a-d) conditions met	STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
☐yes ☐no ☐Met after Allowance Verified and Acknowledged _____ Examiner's Initials _____ Initials	NJ	5	18	6

ADDRESS

ROBERT E KREBS
BURNS DOANE SWECKER & MATHIS
P O BOX 1404
ALEXANDRIA VA 22313-1404

TITLE

METHOD FOR LOGIC OPTIMIZATION FOR IMPROVING TIMING AND CONGESTION DURING PLACEMENT IN INTEGRATED CIRCUIT DESIGN

FILING FEE RECEIVED	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT NO. _____ for the following:	
$583		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

Printed 01/22/2001

SERIAL NUMBER	FILING DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO
09/097,076	06/12/1998	716	2763	032260-004

APPLICANT
SHARAD MALIK, PRINCETON, NEW JERSEY; LAWRENCE PILEGGI, PITTSBURGH, PENNSYLVANIA; ABHIJEET CHAKRABORTY, SUNNYVALE, CALIFORNIA; GARY K YEAP, SAN JOSE, CALIFORNIA; DOUGLAS B BOYLE, PALO ALTO, CALIFORNIA.

CONTINUING DOMESTIC DATA********
VERIFIED

_____

371 (NAT'L STAGE) DATA********
VERIFIED

_____

FOREIGN APPLICATIONS********
VERIFIED

_____

FOREIGN FILING LICENSE GRANTED 07/01/1998 SMALL ENTITY

Foreign priority claimed O yes O no 35 USC 119 (a-d) conditions met O yes O no O Met after Allowance Verified and acknowledged _____ _____ _____ Examiner's Name Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
	CA	5	18	6

ADDRESS
BURNS DOANE SWECKER & MATHIS L L P
POST OFFICE BOX 1404
ALEXANDRIA , VA 22313-1404

TITLE
METHOD FOR LOGIC OPTIMIZATION FOR IMPROVING TIMING AND CONGESTION DURING PLACEMENT IN INTEGRATED CIRCUIT DESIGN

FILING FEE RECEIVED	FEES: Authority has been given in Paper	
$**583	No. _____ to charge/credit DEPOSIT ACCOUNT NO. _____ for the following:	O All Fees O 1.16 Fees (Filing) O 1.17 Fees (Processing Ext. of Time) O 1.18 Fees (Issue) O Other _____ O Credit

1 of 1

JC515 U.S. PTO
06/12/98

"Express Mail" mailing label No. EL086885553US
Date of Deposit June 12, 1998
I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.
Bernardo Caycedo
(Typed or printed name of person mailing paper or fee)

(Signature of person mailing paper or fee)

Patent
Attorney's Docket No. 032260-004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

UTILITY PATENT
APPLICATION TRANSMITTAL LETTER

Box PATENT APPLICATION
Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Enclosed for filing is the utility patent application of Sharad Malik, Lawrence Pileggi, Abhijeet Chakraborty, Gary K. Yeap and Douglas B. Boyle for A METHOD FOR LOGIC OPTIMIZATION FOR IMPROVING TIMING AND CONGESTION DURING PLACEMENT IN INTEGRATED CIRCUIT DESIGN.

Also enclosed are:

[X] 5 sheet(s) of [ ] formal [X] informal drawing(s);

[X] A statement(s) claiming small entity status;

[X] an Assignment document, and Recordation Form cover sheet; and

[X] Other: Postcard.

The declaration of the inventor(s) [X] also is enclosed [ ] will follow.

[ ] Please amend the specification by inserting before the first line the sentence --This application claims priority under 35 U.S.C. §§119 and/or 365 to _____ filed in _____ on _____; the entire content of which is hereby incorporated by reference.--

(01/98)

The filing fee has been calculated as follows [ ] and in accordance with the enclosed preliminary amendment:

CLAIMS					
	NO. OF CLAIMS		EXTRA CLAIMS	RATE	FEE
Basic Application Fee					$790.00
Total Claims	18	MINUS 20 =	0	x $22.00	0
Independent Claims	6	MINUS 3 =	3	x $82.00	246.00
If multiple dependent claims are presented, add $270.00					0
Total Application Fee					1,036.00
If verified Statement claiming small entity status is enclosed, subtract 50% of Total Application Fee					518.00
Add Assignment Recording Fee of $40.00 if Assignment document is enclosed					40.00
TOTAL APPLICATION FEE DUE					$558.00

no fee enclosed

[X] A check in the amount of $ ~~558.00~~ is enclosed for the fee due.

[ ] Charge $ _____ to Deposit Account No. 02-4800 for the fee due.

Please address all correspondence concerning the present application to:

Robert E. Krebs
Burns, Doane, Swecker & Mathis, L.L.P.
P.O. Box 1404
Alexandria, Virginia 22313-1404.

The Commissioner is hereby authorized to charge any appropriate fees under 37 C.F.R. §§ 1.16, 1.17 and 1.21 that may be required by this paper, and to credit any overpayment, to Deposit Account No. 02-4800. This paper is submitted in triplicate.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

Date: June 12, 1998

By: _____
Michael J. Ure
Registration No. 33,089

P.O. Box 1404
Alexandria, Virginia 22313-1404
(650) 854-7400

(01/98)

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO./TITLE

DATE MAILED:

NOTICE TO FILE MISSING PARTS OF APPLICATION
Filing Date Granted

An Application Number and Filing Date have been assigned to this application. The items indicated below, however, are missing. Applicant is given TWO MONTHS FROM THE DATE OF THIS NOTICE within which to file all required items and pay fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a). **If any of items 1 or 3 through 5 are indicated as missing, the SURCHARGE set forth in 37 CFR 1.16(e) of ☐ $65.00 for a small entity in compliance with 37 CFR 1.27, or ☐ $130.00 for a non-small entity, must also be timely submitted in reply to this NOTICE to avoid abandonment.**

If all required items on this form are filed within the period set above, the total amount owed by applicant as a ☐ small entity (statement filed) ☐ non-small entity is $_____.

☐ 1. The statutory basic filing fee is:
- ☐ missing.
- ☐ insufficient.

Applicant must submit $ _____ to complete the basic filing fee and/or file a small entity statement claiming such status (37 CFR 1.27).

☐ 2. Additional claim fees of $_____, including any multiple dependent claim fees, are required.

$_____ for _____ independent claims over 3.

$_____ for _____ dependent claims over 20.

$_____ for multiple dependent claim surcharge.

Applicant must either submit the additional claim fees or cancel additional claims for which fees are due.

☐ 3. The oath or declaration:
- ☐ is missing or unexecuted.
- ☐ does not cover the newly submitted items.
- ☐ does not identify the application to which it applies.
- ☐ does not include the city and state or foreign country of applicant's residence.

An oath or declaration in compliance with 37 CFR 1. 63, including residence information and identifying the application by the above Application Number and Filing Date is required.

☐ 4. The signature(s) to the oath or declaration is/are by a person other than inventor or person qualified under 37 CFR 1.42, 1.43 or 1.47.
A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.

☐ 5. The signature of the following joint inventor(s) is missing from the oath or declaration:

_____

An oath or declaration in compliance with 37 CFR 1.63 listing the names of all inventors and signed by the omitted inventor(s), identifying this application by the above Application Number and Filing Date, is required.

☐ 6. A $50.00 processing fee is required since your check was returned without payment (37 CFR 1.21(m)).

☐ 7. Your filing receipt was mailed in error because your check was returned without payment.

☐ 8. The application does not comply with the Sequence Rules.
See attached "Notice to Comply with Sequence Rules 37 CFR 1.821-1.825."

☐ 9. OTHER: _____

Direct the reply and any questions about this notice to "Attention: Box Missing Parts."

A copy of this notice MUST be returned with the reply.

Customer Service Center
Initial Patent Examination Division (703) 308-1202

FORM PTO-1533 (REV.9-97)

07/28/98 T5567 U.S. PTO

COMBINED DECLARATION AND POWER OF ATTORNEY FOR UTILITY PATENT APPLICATION	Attorney's Docket No. 032260-004

As a below-named inventor, I hereby declare that:
My residence, post office address and citizenship are as stated below next to my name;
I BELIEVE I AM THE ORIGINAL, FIRST AND SOLE INVENTOR (if only one name is listed below) OR AN ORIGINAL, FIRST AND JOINT INVENTOR (if more than one name is listed below) OF THE SUBJECT MATTER WHICH IS CLAIMED AND FOR WHICH A PATENT IS SOUGHT ON THE INVENTION ENTITLED:

A METHOD FOR LOGIC OPTIMIZATION FOR IMPROVING TIMING AND CONGESTION DURING PLACEMENT IN INTEGRATED CIRCUIT DESIGN

the specification of which

(check one) ☒ is attached hereto;
☐ was filed on _____ as
Application No. _____
and was amended on _____ (if applicable);

I HAVE REVIEWED AND UNDERSTAND THE CONTENTS OF THE ABOVE-IDENTIFIED SPECIFICATION, INCLUDING THE CLAIMS, AS AMENDED BY ANY AMENDMENT REFERRED TO ABOVE;

I ACKNOWLEDGE THE DUTY TO DISCLOSE TO THE OFFICE ALL INFORMATION KNOWN TO ME TO BE MATERIAL TO PATENTABILITY AS DEFINED IN TITLE 37, CODE OF FEDERAL REGULATIONS, Sec. 1.56 (as amended effective March 16, 1992);

I do not know and do not believe the said invention was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to said application; that said invention was not in public use or on sale in the United States of America more than one year prior to said application; that said invention has not been patented or made the subject of an inventor's certificate issued before the date of said application in any country foreign to the United States of America on any application filed by me or my legal representatives or assigns more than twelve months prior to said application;

I hereby claim foreign priority benefits under Title 35, United States Code Sec. 119 and/or Sec. 365 of any foreign application(s) for patent or inventor's certificate as indicated below and have also identified below any foreign application for patent or inventor's certificate on this invention having a filing date before that of the application(s) on which priority is claimed:

COMBINED DECLARATION AND POWER OF ATTORNEY			Attorney's Docket No. 032260-004
COUNTRY/INTERNATIONAL	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED
			YES_ NO_
			YES_ NO_

I hereby appoint the following attorneys and agent(s) to prosecute said application and to transact all business in the Patent and Trademark Office connected therewith and to file, prosecute and to transact all business in connection with international applications directed to said invention:

William L. Mathis	17,337	Robert G. Mukai	28,531	Bruce J. Boggs, Jr.	32,344
Peter H. Smolka	15,913	George A. Hovanec, Jr.	28,223	William H. Benz	25,952
Robert S. Swecker	19,885	James A. LaBarre	28,632	Peter K. Skiff	31,917
Platon N. Mandros	22,124	E. Joseph Gess	28,510	Richard J. McGrath	29,195
Benton S. Duffett, Jr.	22,030	R. Danny Huntington	27,903	Matthew L. Schneider	32,814
Joseph R. Magnone	24,259	Eric H. Weisblatt	30,505	Michael G. Savage	32,596
Norman H. Stepno	22,716	James W. Peterson	26,057	Gerald F. Swiss	30,113
Ronald L. Grudziecki	24,970	Teresa Stanek Rea	30,427	Michael J. Urc	33,089
Frederick G. Michaud, Jr.	26,003	Robert E. Krebs	25,885	Charles F. Wieland III	33,096
Alan E. Kopecki	25,813	Robert M. Schulman	31,196	Bruce T. Wieder	33,815
Regis E. Slutter	26,999	William C. Rowland	30,888	Todd R. Walters	34,040
Samuel C. Miller, III 27,360		T. Gene Dillahunty	29,423		
Ralph L. Freeland, Jr.	16,110	Patrick C. Keane	32,858		

and: _____

Address all correspondence to: Robert E. Krebs
BURNS, DOANE, SWECKER & MATHIS, L.L.P.
P.O. Box 1404
Alexandria, Virginia 22313-1404

Address all telephone calls to: Michael J. Urc at (630) 854-7400.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

FULL NAME OF SOLE OR FIRST INVENTOR	SIGNATURE	DATE
Sharad Malik		
RESIDENCE	CITIZENSHIP	
40 Western Way, Princeton, NJ 08540, United States of America	India	
POST OFFICE ADDRESS		
40 Western Way, Princeton, NJ 08540, United States of America		
FULL NAME OF SECOND JOINT INVENTOR, IF ANY	SIGNATURE	DATE
Lawrence Pileggi	[signature]	6/12/98
RESIDENCE	CITIZENSHIP	
357 Dorseyville Road, Pittsburgh, PA 15215, United States of America	United States of America	
POST OFFICE ADDRESS		
357 Dorseyville Road, Pittsburgh, PA 15215, United States of America		
FULL NAME OF THIRD JOINT INVENTOR, IF ANY	SIGNATURE	DATE
Abhijeet Chakraborty		
RESIDENCE	CITIZENSHIP	
710 Dorshire Way, Sunnyvale, CA 94087, United States of America	India	
POST OFFICE ADDRESS		
710 Dorshire Way, Sunnyvale, CA 94087, United States of America		

COMBINED DECLARATION AND POWER OF ATTORNEY		Attorney's Docket No. 032260-004
FULL NAME OF FOURTH JOINT INVENTOR, IF ANY Gary K. Yeap	SIGNATURE	DATE
RESIDENCE 3406 Grossmont Drive, San Jose, CA 95132, United States of America		CITIZENSHIP Malaysia
POST OFFICE ADDRESS 3406 Grossmont Drive, San Jose, CA 95132, United States of America		
FULL NAME OF FIFTH JOINT INVENTOR, IF ANY Douglas B. Boyle	SIGNATURE	DATE
RESIDENCE 385 Calcaterra Place, Palo Alto, CA 94306, United States of America		CITIZENSHIP United States of America
POST OFFICE ADDRESS 385 Calcaterra Place, Palo Alto, CA 94306, United States of America		

07/28/98 Jc567 U.S. PTO

COMBINED DECLARATION AND POWER OF ATTORNEY FOR UTILITY PATENT APPLICATION	Attorney's Docket No. 032260-004

As a below-named inventor, I hereby declare that:
My residence, post office address and citizenship are as stated below next to my name;
I BELIEVE I AM THE ORIGINAL, FIRST AND SOLE INVENTOR (if only one name is listed below) OR AN ORIGINAL, FIRST AND JOINT INVENTOR (if more than one name is listed below) OF THE SUBJECT MATTER WHICH IS CLAIMED AND FOR WHICH A PATENT IS SOUGHT ON THE INVENTION ENTITLED:

A METHOD FOR LOGIC OPTIMIZATION FOR IMPROVING TIMING AND CONGESTION DURING PLACEMENT IN INTEGRATED CIRCUIT DESIGN

the specification of which

(check one) ☒ is attached hereto;
☐ was filed on _____ as
Application No. _____
and was amended on _____ (if applicable);

I HAVE REVIEWED AND UNDERSTAND THE CONTENTS OF THE ABOVE-IDENTIFIED SPECIFICATION, INCLUDING THE CLAIMS, AS AMENDED BY ANY AMENDMENT REFERRED TO ABOVE;

I ACKNOWLEDGE THE DUTY TO DISCLOSE TO THE OFFICE ALL INFORMATION KNOWN TO ME TO BE MATERIAL TO PATENTABILITY AS DEFINED IN TITLE 37, CODE OF FEDERAL REGULATIONS, Sec. 1.56 (as amended effective March 16, 1992);

I do not know and do not believe the said invention was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to said application; that said invention was not in public use or on sale in the United States of America more than one year prior to said application; that said invention has not been patented or made the subject of an inventor's certificate issued before the date of said application in any country foreign to the United States of America on any application filed by me or my legal representatives or assigns more than twelve months prior to said application;

I hereby claim foreign priority benefits under Title 35, United States Code Sec. 119 and/or Sec. 365 of any foreign application(s) for patent or inventor's certificate as indicated below and have also identified below any foreign application for patent or inventor's certificate on this invention having a filing date before that of the application(s) on which priority is claimed:

COMBINED DECLARATION AND POWER OF ATTORNEY	Attorney's Docket No. 032260-004

COUNTRY/INTERNATIONAL	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED
			YES_ NO_
			YES_ NO_

I hereby appoint the following attorneys and agent(s) to prosecute said application and to transact all business in the Patent and Trademark Office connected therewith and to file, prosecute and to transact all business in connection with international applications directed to said invention:

William L. Mathis	17,337	Robert G. Mukai	28,531	Bruce J. Boggs, Jr.	32,344
Peter H. Smolka	15,913	George A. Hovanec, Jr.	28,223	William H. Benz	25,952
Robert S. Swecker	19,885	James A. LaBarre	28,632	Peter K. Skiff	31,917
Platon N. Mandros	22,124	E. Joseph Gess	28,510	Richard J. McGrath	29,195
Benton S. Duffett, Jr.	22,030	R. Danny Huntington	27,909	Matthew L. Schneider	32,814
Joseph K. Magnone	24,239	Eric H. Weisblatt	30,505	Michael G. Savage	32,596
Norman H. Stepno	22,716	James W. Peterson	26,057	Gerald F. Swiss	30,113
Ronald L. Grudziecki	24,970	Teresa Stanek Rea	30,427	Michael J. Ure	33,089
Frederick G. Michaud, Jr.	26,003	Robert B. Krebs	25,885	Charles P. Wieland III	33,096
Alan E. Kopecki	25,813	Robert M. Sobulman	31,196	Bruce T. Wieder	33,815
Regis B. Slutter	26,999	William C. Rowland	30,888	Todd R. Walters	34,040
Samuel C. Miller, III 27,360		T. Gene Dillahunty	25,423		
Ralph L. Freeland, Jr.	16,110	Patrick C. Keane	32,858		

and: _____

Address all correspondence to: Robert B. Krebs
BURNS, DOANE, SWECKER & MATHIS, L.L.P.
P.O. Box 1404
Alexandria, Virginia 22313-1404

Address all telephone calls to: Michael J. Ure at (650) 854-7400.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

FULL NAME OF SOLE OR FIRST INVENTOR	SIGNATURE	DATE
Sharad Malik	Sharad Malik	6/12/98
RESIDENCE		CITIZENSHIP
40 Western Way, Princeton, NJ 08540, United States of America		India
POST OFFICE ADDRESS		
40 Western Way, Princeton, NJ 08540, United States of America		
FULL NAME OF SECOND JOINT INVENTOR, IF ANY	SIGNATURE	DATE
Lawrence Pileggi		
RESIDENCE		CITIZENSHIP
357 Dorseyville Road, Pittsburgh, PA 15215, United States of America		United States of America
POST OFFICE ADDRESS		
357 Dorseyville Road, Pittsburgh, PA 15215, United States of America		
FULL NAME OF THIRD JOINT INVENTOR, IF ANY	SIGNATURE	DATE
Abhijeet Chakraborty	Abhijeet Chakraborty	6/12/98
RESIDENCE		CITIZENSHIP
710 Dorshire Way, Sunnyvale, CA 94087, United States of America		India
POST OFFICE ADDRESS		
710 Dorshire Way, Sunnyvale, CA 94087, United States of America		

COMBINED DECLARATION AND POWER OF ATTORNEY		Attorney's Docket No. 032260-004
FULL NAME OF FOURTH JOINT INVENTOR, IF ANY Gary K. Yeap	SIGNATURE	DATE 6-12-98
RESIDENCE 3406 Grossmont Drive, San Jose, CA 95132, United States of America		CITIZENSHIP Malaysia
POST OFFICE ADDRESS 3406 Grossmont Drive, San Jose, CA 95132, United States of America		
FULL NAME OF FIFTH JOINT INVENTOR, IF ANY Douglas B. Boyle	SIGNATURE Douglas B. Boyle	DATE 6/12/98
RESIDENCE 385 Calcaterra Place, Palo Alto, CA 94306, United States of America		CITIZENSHIP United States of America
POST OFFICE ADDRESS 385 Calcaterra Place, Palo Alto, CA 94306, United States of America		

07/28/98 Jc567 U.S. PTO

Patent
Attorney's Docket No. 032260-004

Applicant or Patentee: Sharad Malik, et al.

Application or Patent No.: Unassigned

Filed or Issued: On even date herewith

For: A METHOD FOR LOGIC OPTIMIZATION FOR IMPROVING TIMING AND CONGESTION DURING PLACEMENT IN INTEGRATED CIRCUIT DESIGN

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS (37 C.F.R. §§ 1.9(f) AND 1.27(c)) - SMALL BUSINESS CONCERN

I hereby declare that I am

[ ] the owner of the small business concern identified below:
[X] an official of the small business concern empowered to act on behalf of the concern identified below:

NAME OF CONCERN MONTEREY DESIGN SYSTEMS

ADDRESS OF CONCERN 894 Ross Drive, Suite 203

Sunnyvale, California 94089-1443

I hereby declare that the above-identified small business concern qualifies as a small business concern as defined in 13 C.F.R. § 1.21 for purposes of paying reduced fees under Sections 41(a) and 41(b) of Title 35, United States Code, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average, over the previous fiscal year of the concern, of the persons employed on a full-time, part-time, or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention entitled A METHOD FOR LOGIC OPTIMIZATION FOR IMPROVING TIMING AND CONGESTION DURING PLACEMENT IN INTEGRATED CIRCUIT DESIGN by inventor(s) Sharad Malik, Lawrence Pileggi, Abhijeet Chakraborty, Gary K. Yeap, and Douglas B. Boyle described in

[X] the specification filed herewith
[ ] Application No. _____, filed _____.
[ ] Patent No. _____, issued _____.

If the rights held by the above-identified small business concern are not exclusive, each individual, concern, or organization having rights to the invention is listed below,* and no rights to the invention are held by any person, other than the inventor, who would not qualify as an independent inventor under 37 C.F.R. § 1.9(c), or by any concern that would not qualify as either a small business concern under 37 C.F.R. § 1.9(d) or a nonprofit organization under 37 C.F.R. § 1.9(e).

*NOTE: Separate verified statements are required from each named person, concern, or organization having rights to the invention averring to their status as small entities. (37 C.F.R. § 1.27.)

(9/98)

Application No. Unassigned
Attorney's Docket No. 032260-004

NAME _____

ADDRESS _____

[ ] individual [ ] small business concern [ ] nonprofit organization

NAME _____

ADDRESS _____

[ ] individual [ ] small business concern [ ] nonprofit organization

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earlier of the issue fee and any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 C.F.R. § 1.28(b).)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code; and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

NAME OF PERSON SIGNING Douglas B. Boyle

TITLE OF PERSON OTHER THAN OWNER Vice President

ADDRESS OF PERSON SIGNING 894 Ross Drive, Suite 203

Sunnyvale, California 94089-1443

SIGNATURE Douglas B. Boyle DATE 6/12/98

Section 5

Patent
Attorney's Docket No. 032260-004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	
Sharad Malik, et al.	Group Art Unit: 2773
Application No.: 09/097,076	Examiner: Unassigned
Filed: June 12, 1998	
For: METHOD FOR LOGIC OPTIMIZATION FOR IMPROVING TIMING AND CONGESTION DURING PLACEMENT IN INTEGRATED CIRCUIT DESIGN	

TRANSMITTAL LETTER FOR MISSING PARTS OF APPLICATION

BOX: MISSING PART
Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In complete response to the Notice to File Missing Parts of Application Under 37 C.F.R. § 1.53(e) dated July 6, 1998, enclosed please find:

[X] a Combined Declaration and Power of Attorney signed by the inventor(s) and the surcharge of [X] $65.00 [ ] $130.00 as set forth in 37 C.F.R. § 1.16(e);

[ ] Note that the inventor(s) identified on the currently filed Combined Declaration and Power of Attorney are different than listed on the application filing papers.

[X] a Declaration Claiming Small Entity Status;

[ ] a Petition for Extension of Time;

[ ] a verified English translation of the Application, and the $130.00 fee as set forth in 37 C.F.R. § 1.17(k);

[ ] an Assignment document and the $40.00 Assignment Recording Fee;

[X] other a postcard;

[X] a check in the amount of $ 583.00 for the fee due; and

[ ] charge $_____ to Deposit Account No.02-4800 for the fee due.

(12/97)

The Commissioner is hereby authorized to charge any appropriate fees under 37 C.F.R. §§ 1.16, 1.17 and 1.21 that may be required by this paper, and to credit any overpayment, to Deposit Account No. 02-4800. This paper is submitted in triplicate.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

P.O. Box 1404
Alexandria, Virginia 22313-1404
(650) 854-7400

By: _____
Michael J. Ure
Registration No. 33,089

Date: July 27, 1998

(12/97)

07/28/98 JC567 U.S. PTO

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO./TITLE
09/123,726	07/28/98	MARLIN	

ROBERT E KREBS
BURNS DOANE SWECKER & MATHIS
P O BOX 1404
ALEXANDRIA VA 22313-1404

DATE MAILED: 07/08/98

NOTICE TO FILE MISSING PARTS OF APPLICATION

Filing Date Granted

An Application Number and Filing Date have been assigned to this application. The items indicated below, however, are missing. Applicant is given TWO MONTHS FROM THE DATE OF THIS NOTICE within which to file all required items and pay fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a). **If any of items 1 or 3 through 5 are indicated as missing, the SURCHARGE set forth in 37 CFR 1.16(e) of ☐ $65.00 for a small entity in compliance with 37 CFR 1.27, or ☐ $130.00 for a non-small entity, must also be timely submitted in reply to this NOTICE to avoid abandonment.**

If all required items on this form are filed within the period set above, the total amount owed by applicant as a ☐ small entity (statement filed) ☐ non-small entity is $ 710.

☑ 1. The statutory basic filing fee is:
- ☑ missing.
- ☐ insufficient.

Applicant must submit $ 710 to complete the basic filing fee and/or file a small entity statement claiming such status (37 CFR 1.27).

☐ 2. Additional claim fees of $_____, including any multiple dependent claim fees; are required.

$_____ for _____ independent claims over 3.

$_____ for _____ dependent claims over 20.

$_____ for multiple dependent claim surcharge.

Applicant must either submit the additional claim fees or cancel additional claims for which fees are due.

☑ 3. The oath or declaration:
- ☑ is missing or unexecuted.
- ☑ does not cover the newly submitted items.
- ☐ does not identify the application to which it applies.
- ☐ does not include the city and state or foreign country of applicant's residence.

An oath or declaration in compliance with 37 CFR 1. 63, including residence information and identifying the application by the above Application Number and Filing Date is required.

☐ 4. The signature(s) to the oath or declaration is/are by a person other than inventor or person qualified under 37 CFR 1.42, 1.43 or 1.47.

A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.

08/03/1998 DTHOMAS 00000001 09070[illegible]
01 FC:205 65.00 DP
02 FC:201 395.00 DP
03 FC:202 123.00 DP

☐ 5. The signature of the following joint inventor(s) is missing from the oath or declaration:

_____

An oath or declaration in compliance with 37 CFR 1.63 listing the names of all inventors and signed by the omitted inventor(s), identifying this application by the above Application Number and Filing Date, is required.

☐ 6. A $50.00 processing fee is required since your check was returned without payment (37 CFR 1.21(m)).

☐ 7. Your filing receipt was mailed in error because your check was returned without payment.

☐ 8. The application does not comply with the Sequence Rules.

See attached "Notice to Comply with Sequence Rules 37 CFR 1.821-1.825."

☐ 9. OTHER: _____

Direct the reply and any questions about this notice to "Attention: Box Missing Parts."

A copy of this notice MUST be returned with the reply.

03.2260-004

Customer Service Center
Initial Patent Examination Division (703) 308-1202

PART 2 - COPY TO BE RETURNED WITH RESPONSE

FORM PTO-1533 (REV 9-97)

Decl & Trans & Filing Fee Due 9/6/98

OIPE JC4 AUG 20 1998 PATENT & TRADEMARK OFFICE

#4

Patent
Attorney's Docket No. 032260004

RECEIVED SEP 15 PM 9:56 GROUP 2700

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)	**ATTENTION: APPLICATIONS BRANCH**
Sharad Malik, et al.	)	
Application No.: 09/097,076	)	Group Art Unit: 2773
Filed: June 12, 1998	)	Examiner: Unassigned
For: METHOD FOR LOGIC OPTIMIZATION FOR IMPROVING TIMING AND CONGESTION DURING PLACEMENT IN INTEGRATED CIRCUIT DESIGN	)	

REQUEST FOR CORRECTED OFFICIAL FILING RECEIPT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Enclosed is a copy of the "corrected" Official Filing Receipt marked in red to show corrections that are needed. Three corrections were requested, but only one correction was made on this document. The remaining two corrections are as follows.

1. **Last inventor's residence should be "PALO ALTO" INSTEAD OF "PALOALTO".**
2. **Seventh word of title should be "TIMING" instead of "TIMMING".**

Issuance of a corrected Official Filing Receipt is respectfully requested.

[X] This Request for Corrected Official Filing Receipt is being filed to correct a Patent Office error. No fee is required.

[ ] The $25.00 fee required under 37 C.F.R. § 1.19(h) to correct an Official Filing Receipt due to applicant error: [ ] is enclosed; [ ] is authorized to be charged to Deposit Account No. 02-4800 and this paper is submitted in triplicate.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

RECEIVED 98 SEP 22 PM 2:05 GROUP 2700

By: Michael J. Ure
Michael J. Ure
Registration No. 33,089

P.O. Box 1404
Alexandria, VA 22313-1404
(650) 854-7400

Date: July 27, 1998

(10/97)

PTO-103X
(Rev. 8-96)

FILING RECEIPT

CORRECTED

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
ASSISTANT SECRETARY AND COMMISSIONER
OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING DATE	GRP ART UNIT	FIL FEE REC'D	ATTORNEY DOCKET NO.	DRWGS	TOT CL	IND CL
09/097,076	06/12/98	2773	$583.00	032260-004	6	18	6

ROBERT E KREBS
BURNS DOANE SWECKER & MATHIS
P O BOX 1404
ALEXANDRIA VA 22313-1404

Receipt is acknowledged of this nonprovisional Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Application Processing Division's Customer Correction Branch within 10 days of receipt. Please provide a copy of the Filing Receipt with the changes noted thereon.

Applicant(s)

SHARAD MALIK, PRINCETON, NJ; LAWRENCE PILEGGI, PITTSBURGH, PA; ABHIJEET CHAKRABORTY, SUNNYVALE, CA; GARY K. YEAP, SAN JOSE, CA; DOUGLAS B. BOYLE, ~~PALOALTO~~ PALO ALTO, CA.

FOREIGN FILING LICENSE GRANTED 07/01/98 * SMALL ENTITY *

TITLE

METHOD FOR LOGIC OPTIMIZATION FOR IMPROVING ~~TIMMING~~ TIMING AND CONGESTION DURING PLACEMENT IN INTEGRATED CIRCUIT DESIGN

PRELIMINARY CLASS: 345

BURNS, DOANE, SWECKER & MATHIS, L.L.P.
RECEIVED
AUG 19 1998
DOCKETED
032260 004
MSL

(see reverse)

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
ASSISTANT SECRETARY AND COMMISSIONER
OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

DATE: 4/4/96

FROM: CUSTOMER CORRECTIONS
APPLICATION DIVISION
LOC. 0380

SUBJ.: APPLICATION FILES NEEDED
FOR CORRECTION/UPDATE

GROUP ART UNIT: 2713

APPLICATION NUMBER 08/097,076 IS NEEDED IMMEDIATELY FOR CORRECTION.

PLEASE ATTACH THIS FORM TO THE ABOVE APPLICATION AND RETURN IT TO THE APPLICATION PROCESSING DIVISION, CUSTOMER CORRECTIONS CP2-6C17.

IF YOU ARE UNABLE TO LOCATE THE APPLICATION OR HAVE A QUESTION, PLEASE CALL ME AT 308-1202.

THANK YOU FOR YOUR ASSISTANCE

DORA STROUD
SUPERVISOR

OIPE
JUL 28 1998
PATENT & TRADEMARK OFFICE

Patent
Attorney's Docket No. 032260-004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)	**ATTENTION: APPLICATIONS BRANCH**
Sharad Malik, et al.	)	
Application No.: 09/097,076	)	Group Art Unit: 2773
Filed: June 12, 1998	)	Examiner: Unassigned
For: METHOD FOR LOGIC OPTIMIZATION FOR IMPROVING TIMING AND CONGESTION DURING PLACEMENT IN INTEGRATED CIRCUIT DESIGN	)	

RECEIVED
98 AUG -7 AM 8:57
GROUP 2700

REQUEST FOR CORRECTED OFFICIAL FILING RECEIPT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Enclosed is a copy of the Official Filing Receipt marked in red to show corrections that are needed. The corrections are as follows.

Last inventor's residence should be "PALO ALTO" INSTEAD OF "PALOALTO".

First two words of title should be "METHOD FOR" instead of "METHODFOR".

Seventh word of title should be "TIMING" instead of "TIMMING".

Issuance of a corrected Official Filing Receipt is respectfully requested.

[X] This Request for Corrected Official Filing Receipt is being filed to correct a Patent Office error. No fee is required.

[ ] The $25.00 fee required under 37 C.F.R. § 1.19(h) to correct an Official Filing Receipt due to applicant error: [ ] is enclosed; [ ] is authorized to be charged to Deposit Account No. 02-4800 and this paper is submitted in triplicate.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

By: _____
Michael J. Ure
Registration No. 33,089

P.O. Box 1404
Alexandria, VA 22313-1404
(650) 854-7400

Date: July 27, 1998

(10/97)

PTO-103X
(Rev. 8-95)

FILING RECEIPT

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
ASSISTANT SECRETARY AND COMMISSIONER
OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING DATE	GRP ART UNIT	FIL FEE REC'D	ATTORNEY DOCKET NO.	DRWGS	TOT CL	IND CL
09/097,076	06/12/98	2773	$0.00	032260-004	5	18	6

ROBERT E KREBS
BURNS DOANE SWECKER & MATHIS
P O BOX 1404
ALEXANDRIA VA 22313-1404

Receipt is acknowledged of this nonprovisional Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Application Processing Division's Customer Correction Branch within 10 days of receipt. Please provide a copy of this Filing Receipt with the changes noted thereon.

Applicant(s)

SHARAD MALIK, PRINCETON, NJ; LAWRENCE PILEGGI, PITTSBURGH, PA; ABHIJEET CHAKRABORTY, SUNNYVALE, CA; GARY K YEAP, SAN JOSE, CA; DOUGLAS B BOYLE, ~~PALOALTO~~ PALO ALTO, CA.

FOREIGN FILING LICENSE GRANTED 07/01/98

TITLE

~~METHODFOR~~ METHOD FOR LOGIC OPTIMIZATION FOR IMPROVING ~~TIMMING~~ TIMING AND CONGESTION DURING PLACEMENT IN INTEGRATED CIRCUIT DESIGN

PRELIMINARY CLASS: 345

032260-004
MJU

BURNS, DOANE, SWECKER & MATHIS, L.L.P.
RECEIVED
JUL 7 1998
LDR
DOCKETED 7-07-98

(see reverse)

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/097,076	06/12/98	MALIK	3 [illegible] 064

LM02/1104

ROBERT E CRERS
BURNS DOANE SWECKER & MATHIS
P O BOX 1404
ALEXANDRIA VA 22313-1404

EXAMINER	
TANG,H	
ART UNIT	PAPER NUMBER
2763	6

DATE MAILED: 11/05/99

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

PTO-90C (Rev. 2/95)

1- File Copy

Office Action Summary

Application No.	Applicant(s)
09/097,076	Malik et al.
Examiner	**Group Art Unit**
Hugh Jones	2763

☒ Responsive to communication(s) filed on *Jun 12, 1998*

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) *1-18* is/are pending in the applicat

Of the above, claim(s) _____ is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-8, 10, and 12-18* is/are rejected.

☒ Claim(s) *9 and 11* is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

— SEE OFFICE ACTION ON THE FOLLOWING PAGES —

U.S. Patent and Trademark Office
PTO-326 (Rev. 9-95) **Office Action Summary** Part of Paper No. 6

DETAILED ACTION

Specification

1. It is noted that this application appears to disclose subject matter at least partially disclosed in prior U. S. Patent 5,557,533 (and for which there is a common inventor, namely Boyle) - there is no acknowledgment in the present application of said patent. Applicant is reminded of the duty of disclosure (Cross-References to Related Applications: See 37 CFR 1.78 and MPEP § 201.11.).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. **Claims 1-3, 6-7, 15 and 17-18 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Koford et al..** Koford et al. discloses: cell placement alteration in order to reduce congestion. As per "logic modification(s)", see col. 26, lines 59-65, and compare to claim 7, wherein, "... *modifying logic comprises replacing an original set of gates with a different set of gates in the circuit that is logically equivalent to the original set of gates.*" See also, abstract; fig. 50 (iterative placement and optimization); col. 15, lines 15-36 (congestion based cost function);

col. 16, lines 8-19; col. 22, lines 4-21; col. 26, lines 59-65 (equivalence - 395/500.05/CCLS); col. 31, line 27 to col. 33, line 4 (congestion); col. 39, line 23 to col. 43, line 67 (congestion and iterative optimization).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 4-5, 8, 12-14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over [Koford et al.] in view of [Dornier et al.] or [Hoshizaki et al] and the taking of official notice.**

6. **Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over [Koford et al.] in view of [Hoshizaki et al] and the taking of official notice.**

7. Koford et al. discloses: cell placement alteration in order to reduce congestion. As per "logic modification(s)", see col. 26, lines 59-65, and compare to claim 7, wherein, "... *modifying logic comprises replacing an original set of gates with a different set of gates in the circuit that is logically equivalent to the original set of gates.*" See also, abstract; fig. 50 (iterative placement and optimization); col. 15, lines 15-36 (congestion based cost function); col. 16, lines 8-19; col.

22, lines 4-21; col. 26, lines 59-65 (equivalence - 395/500.05/CCLS); col. 31, line 27 to col. 33, line 4 (congestion); col. 39, line 23 to col. 43, line 67 (congestion and iterative optimization). Koford et al. does not disclose details concerning a number of other logic modifications which affect timing, number of pins, etc.. As per claim 8, wherein, "... a lower ratio of number of pins to routable area ...", official notice is taken that this would have been obvious to one of ordinary skill in the art at the time of the invention because this is just a restatement of one cause of congestion (the number of pins is related to the number of channels - the higher the channel density, the higher the congestion). Official notice is also taken that logic modifications which result in a speeding up of the circuit or other timing considerations would been obvious to one of ordinary skill in the art at the time of the invention. These teachings were provided by others as per congestion.

8. Dornier et al. discloses details concerning congestion and timing delays. See abstract; col. 2, lines 38-65; col. 3, lines 33-38; col. 4, lines 48-59, wherein, "... The reduction in the number of traces results in a reduction in layout congestion, with a consequent reduction in the length of the traces. The shortened traces in turn reduce signal delays, so that a computer's performance is increased."

9. Hoshizaki et al. discloses the use of logic modification to reduce congestion (col. 5, lines 30-40), thus leading to speed increases (col. 7, lines 50-63). As per claim 10, see col. 7, lines 58-63.

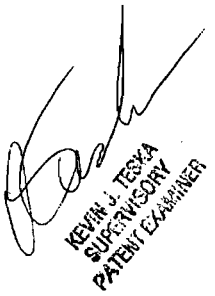
Allowable Subject Matter

10. **Claims 9 and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.**

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Cheng discloses using iterative changes in placement to improve congestion. See fig. 4-6; col. 1-3.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Hugh Jones whose telephone number is (703) 305-0023.



Dr. Hugh Jones

November 3, 1999

Notice of References Cited

Application No.	Applicant(s)		
09/097,076	Malik et al.		
Examiner		Group Art Unit	Page 1 of 1
Hugh Jones		2763	

U.S. PATENT DOCUMENTS

	DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS
A	5,847,965	12/98	Cheng	395	500.09
B	5,557,533	9/96	Koford et al.	706	13
C	5,561,772	10/96	Dorner et al.	710	101
D	5,572,482	11/96	Hoshizaki et al.	365	233
E					
F					
G					
H					
I					
J					
K					
L					
M					

FOREIGN PATENT DOCUMENTS

	DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUBCLASS
N						
O						
P						
Q						
R						
S						
T						

NON-PATENT DOCUMENTS

	DOCUMENT (Including Author, Title, Source, and Pertinent Pages)	DATE
U		
V		
W		
X		

Patent
Attorney's Docket No. 032260-004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)	
	)	
Sharad Malik, et al.	)	Group Art Unit: 2763
	)	
Application No.: 09/097,076	)	Examiner: Jones, H.
	)	
Filed: June 12, 1998	)	
	)	
For: METHOD FOR LOGIC OPTIMIZATION FOR IMPROVING TIMING AND CONGESTION DURING PLACEMENT IN INTEGRATED CIRCUIT DESIGN	)	

OIPE JC83 JAN 21 2000 PATENT & TRADEMARK OFFICE

RECEIVED JAN 24 2000 TC 2700 MAIL ROOM

RESPONSE UNDER 37 C.F.R. 1.111

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

The following remarks are responsive to the Office Action of November 5, 1999.

REMARKS

The Office Action of November 5, 1999 has been carefully considered. Withdrawal of the rejection and allowance of the present application in view of the following remarks is respectfully requested.

Claims 9 and 11 were indicated as containing allowable subject matter, which indication is appreciatively acknowledged.

Claims 1-3, 6-7, 15, 17 and 18 were rejected as being unpatentable over Koford, and claims 4, 5, 8, 10, 12-14 and 16 were rejected as being unpatentable over Koford in

view of one or more secondary references. These rejections are respectfully traversed and reconsideration requested.

The present invention and the primary reference, Koford, share one common reference point, namely the principle of *congestion* in integrated circuits. Both disclosures attempt to relieve congestion, a well-known problem in IC physical design. The manner in which congestion is addressed, however, admits of little similarity between Koford and the present invention.

In Koford, congestion is addressed through *placement modification*, principally through *cell transposition*.

In the present invention, congestion is addressed through *logic modification*. In logic modification, the actual layout of the circuit is changed (e.g., the identities of the cells or interconnections between cells are changed as opposed to mere transposition of cells, or trading places between cells.) However, the identities or interconnections of the cells are changed in such a manner as to maintain logical equivalency between the original circuit and the changed circuit.

Claim 1, which may be regarded as representative of the present claims, recites in part, "performing *logic modifications* within selected bins of the integrated circuit design to allow congestion of the placement to be improved." Examples of suitable logic modifications are shown in Figs. 3(a)-3(c) of the present specification.

Koford et al. does not deal with logic optimizations at all. In column 26, lines 59-65, Koford discusses the addition of dummy or idle cells to the design. But these cells are not connected to any part of the design, and as a consequence the logic circuit for the design is not changed at all. *At no point is a set of logical gates being replaced by a different set of logically equivalent gates.*

Hence, although both disclosures relate generally to congestion and iterative improvement, the manner of improvement, as specifically claimed in the present claims, is entirely different. Furthermore, although much discussion in Koford is centered on congestion as a cost function, such discussion relates entirely to *cell placement* and has absolutely no reference to any *logic optimization*. Accordingly, the claims are not believed to be anticipated by Koford.

Likewise, the subsidiary references contain no hint or suggestion of the use of logic optimizations in reducing congestion.

Dornier et al. (Patent 5,561,772) describes how reduction in the number of traces results in lower congestion and reduced signal delays. The present invention does not claim to reduce signal delays by reducing congestion. Rather, the approach of the present invention is to first reduce signal delays using conventional logic optimization techniques. This reduction in the signal delays provides additional slack that can then be used by a subsequent placement step to relieve congestion. Thus, the present invention uses delay reduction via logic optimization to aid placement, while Dornier et al. uses trace reduction to reduce congestion and get speed reduction as a side benefit. Further, Dornier et al. does not deal with cell-based integrated circuit design (the domain of the present invention), but rather with the input-output bus of a computer system.

Hoshizaki et al. (Patent 5,572,482) describes the design of sense amplifier circuits to reduce congestion in the design of Static RAM. This relates to one very specific circuit design (sense amplifiers) for one very specific component (RAM). Sense amplifiers are analog circuits and not digital logic circuits which is the domain of the present invention. It is not possible to apply the analog circuit design technique described in Hoshizaki to digital logic circuits.

Cheng et al. (Patent 5,847,965) relates to iterative placement to relieve congestion. *It does not deal with any logic optimization steps to help with a subsequent placement step, which is the subject of the present invention.*

Accordingly, claims 1-18 are believed to be allowable. Notice of the same is respectfully requested.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

By: _____
Michael J. Ure
Registration No. 33,089

P.O. Box 1404
Alexandria, Virginia 22313-1404
(650) 622-2300

Date: January 20, 2000

Patent
Attorney's Docket No. 032260-004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)	
	)	
Sharad Malik, et al.	)	**NON-FEE AMENDMENT**
	)	
Application No.: 09/097,076	)	Group Art Unit: 2763
	)	
Filed: June 12, 1998	)	Examiner: Jones, H.
	)	
For: METHOD FOR LOGIC OPTIMIZATION FOR IMPROVING TIMING AND CONGESTION DURING PLACEMENT IN INTEGRATED CIRCUIT DESIGN	)	

OIPE JC63 JAN 21 2000 PATENT & TRADEMARK OFFICE

RECEIVED JAN 24 2000 TC 2100 MAIL ROOM

AMENDMENT/REPLY TRANSMITTAL LETTER

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Enclosed is a reply for the above-identified patent application.

[X] Also enclosed is a return postcard.

[X] No additional claim fee is required.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

By: _____
Michael J. Ure
Registration No. 33,089

P.O. Box 1404
Alexandria, Virginia 22313-1404
(650) 622-2300

Date: January 20, 2000

(09/99)

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/097,076	06/12/98	MALIK S	032260-004

021839
BURNS DOANE SWECKER & MATHIS
P O BOX 1404
ALEXANDRIA VA 22313-1404

LM71/0131

EXAMINER	
JONES,H	

ART UNIT	PAPER NUMBER
2763	8

DATE MAILED: 01/31/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

PTO-90C (Rev. 2/95) 1- File Copy

Notice of Allowability	Application No. 09/097,076	Applicant(s) Malik et al.
	Examiner Hugh Jones	Group Art Unit 2763

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance and Issue Fee Due or other appropriate communication will be mailed in due course.

☒ This communication is responsive to 1/21/2000

☒ The allowed claim(s) is/are 1-18

☐ The drawings filed on _____ are acceptable.

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

A SHORTENED STATUTORY PERIOD FOR RESPONSE to comply with the requirements noted below is set to EXPIRE THREE MONTHS FROM THE "DATE MAILED" of this Office action. Failure to timely comply will result in ABANDONMENT of this application. Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

☐ Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL APPLICATION, PTO-152, which discloses that the oath or declaration is deficient. A SUBSTITUTE OATH OR DECLARATION IS REQUIRED.

☒ Applicant MUST submit NEW FORMAL DRAWINGS

☒ because the originally filed drawings were declared by applicant to be informal.

☐ including changes required by the Notice of Draftsperson's Patent Drawing Review, PTO-948, attached hereto or to Paper No. _____.

☐ including changes required by the proposed drawing correction filed on _____, which has been approved by the examiner.

☐ including changes required by the attached Examiner's Amendment/Comment.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the reverse side of the drawings. The drawings should be filed as a separate paper with a transmittal lettter addressed to the Official Draftsperson.

☐ Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Any response to this letter should include, in the upper right hand corner, the APPLICATION NUMBER (SERIES CODE/SERIAL NUMBER). If applicant has received a Notice of Allowance and Issue Fee Due, the ISSUE BATCH NUMBER and DATE of the NOTICE OF ALLOWANCE should also be included.

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

☐ Interview Summary, PTO-413

☐ Examiner's Amendment/Comment

☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material

☒ Examiner's Statement of Reasons for Allowance

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER

U. S. Patent and Trademark Office
PTO-37 (Rev. 9-95) **Notice of Allowability** Part of Paper No. 8

DETAILED ACTION

Allowable Subject Matter

1. Claims 1-18 are allowed.

2. The application having been allowed, formal drawings are required in response to this Office action.

3. The following is an examiner's statement of reasons for allowance: Applicant's remarks concerning the prior art (pp. 2-3 of paper # 7) are persuasive. In particular, as pointed out by Applicant, Koford et al. primarily teaches placement modification. This is demonstrated by the disclosure in col. 41, line 55 to col. 42, line 50, wherein the cost function (lines 45-48 of col. 42) consists of placement criteria instead of logic modifications in order to reduce congestion. An updated search uncovered one reference which shoud be discussed, namely Hong et al.. This patent teaches the effects of logic modification on congestion (see, for example col. 25-26). However, it is clear (see col. 40) that there is no teaching of specifically carrying out logic optimization *in order to reduce* congestion. The examiner would argue that it would be obvious that there is a relationship between logic arrangement and congestion; however, the prior art does not disclose specifically carrying out logic optimization *in order to reduce* congestion.

4. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Hugh Jones whose telephone number is (703) 305-0023.

Dr. Hugh Jones

January 25, 2000

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER

Notice of References Cited

Application No.	Applicant(s)		
09/097,076	Malik et al.		
Examiner		Group Art Unit	Page 1 of 1
Hugh Jones		2763	

U.S. PATENT DOCUMENTS

		DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS
	A	4,464,292	11/1984	Hong et al.	716	13
	B					
	C					
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FOREIGN PATENT DOCUMENTS

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NON-PATENT DOCUMENTS

		DOCUMENT (Including Author, Title, Source, and Pertinent Pages)	DATE
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	X		

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

NOTICE OF ALLOWANCE AND ISSUE FEE DUE

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED

First Named Applicant		35 USC 154(b) term ext.	days.

TITLE OF INVENTION

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED.

THE ISSUE FEE MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED.

HOW TO RESPOND TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.
If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is changed, pay twice the amount of the FEE DUE shown above and notify the Patent and Trademark Office of the change in status, or
B. If the status is the same, pay the FEE DUE shown above.

If the SMALL ENTITY is shown as NO:

A. Pay FEE DUE shown above, or

B. File verified statement of Small Entity Status before, or with, payment of 1/2 the FEE DUE shown above.

II. Part B-Issue Fee Transmittal should be completed and returned to the Patent and Trademark Office (PTO) with your ISSUE FEE. Even if the ISSUE FEE has already been paid by charge to deposit account, Part B Issue Fee Transmittal should be completed and returned. If you are charging the ISSUE FEE to your deposit account, section "4b" of Part B-Issue Fee Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give application number and batch number.
Please direct all communications prior to issuance to Box ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PATENT AND TRADEMARK OFFICE COPY

PTOL-85 (REV. 10-96) Approved for use through 06/30/99. (0651-0033)

PART B—ISSUE FEE TRANSMITTAL

Complete and mail this form, together with applicable fees, to: **Box ISSUE FEE**
Assistant Commissioner for Patents
Washington, D.C. 20231

OIPE APR 28 2000 JC35 PATENT & TRADEMARK OFFICE

7640 5/11/00

MAILING INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE. Blocks 1 through 4 should be completed where appropriate. All further correspondence including the Issue Fee Receipt, the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

Note: The certificate of mailing below can only be used for domestic mailings of the Issue Fee Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing.

Certificate of Mailing

I hereby certify that this Issue Fee Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Box Issue Fee address above on the date indicated below.

(Depositor's name)

(Signature)

(Date)

CURRENT CORRESPONDENCE ADDRESS (Note: Legibly mark-up with any corrections or use Block 1)

021839 LM71/0131
BURNS DOANE SWECKER & MATHIS
P O BOX 1404
ALEXANDRIA VA 22313-1404

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT		DATE MAILED
09/097,076	06/12/98	018	JONES, H	2763	01/31/00

First Named Applicant		
MALIK,	35 USC 154(b) term ext. =	0 Days.

TITLE OF INVENTION: METHOD FOR LOGIC OPTIMIZATION FOR IMPROVING TIMING AND CONGESTION DURING PLACEMENT IN INTEGRATED CIRCUIT DESIGN

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
2 032260-004	716-009.000	H44	UTILITY	YES	$605.00	05/01/00

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363). Use of PTO form(s) and Customer Number are recommended, but not required.

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47) attached.

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Burns Doane Swecker
2 & Mathis L.L.P
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)
PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the PTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: MONTEREY DESIGN SYSTEMS

(B) RESIDENCE: (CITY & STATE OR COUNTRY): Sunneyvale, California

Please check the appropriate assignee category indicated below (will not be printed on the patent)
☐ Individual ☒ corporation or other private group entity ☐ government

4a. The following fees are enclosed (make check payable to Commissioner of Patents and Trademarks):
☒ Issue Fee
☒ Advance Order - # of Copies 10

4b. The following fees or deficiency in these fees should be charged to:
DEPOSIT ACCOUNT NUMBER 02-4800
(ENCLOSE AN EXTRA COPY OF THIS FORM)
☐ Issue Fee
☐ Advance Order - # of Copies

The COMMISSIONER OF PATENTS AND TRADEMARKS IS requested to apply the Issue Fee to the application identified above.

(Authorized Signature) (Date) 4/28/00

NOTE: The Issue Fee will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the Patent and Trademark Office. Robert E. Krebs, Reg. No. 25,885

05/01/2000 KZEWDIE1 00000104 09097076
01 FC:242 605.00 OP
02 FC:561 30.00 OP

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending on the needs of the individual case. Any comments on the amount of time required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, D.C. 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND FEES AND THIS FORM TO: Box Issue Fee, Assistant Commissioner for Patents, Washington D.C. 20231

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMIT THIS FORM WITH FEE

CERTIFICATE OF FACSIMILE TRANSMISSION

I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS BEING FACSIMILE TRANSMITTED TO EXAMINER, HUGH JONES, ART UNIT 2763, U.S. PATENT AND TRADEMARK OFFICE ON THE DATE SHOWN BELOW.

Name of person signing certification: Sharon E. Byam

Date: March 7, 2000 Signature: Sharon E. Byam

Refaxed April 18, 2000 Sharon E. Byam

Patent

Attorney's Docket No. 032260-004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)	**BOX AF**
	)	
Sharad Malik, et al.	)	Group Art Unit: 2763
	)	
Application No.: 09/097,076	)	Examiner: Jones, H.
	)	
Filed: June 12, 1998	)	
	)	
For: METHOD FOR LOGIC OPTIMIZATION FOR IMPROVING TIMING AND CONGESTION DURING PLACEMENT IN INTEGRATED CIRCUIT DESIGN	)	

AMENDMENT UNDER 37 C.F.R. §312

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Please amend this application as follows:

IN THE CLAIMS:

1. A method of modifying an integrated circuit design to facilitate placement of circuit elements within one or more regions called bins on an integrated circuit design grid, comprising the steps of:

performing an initial placement of integrated circuit elements within bins on the design grid;

calculating congestion of the initial placement; and

a1

subject to limits on the increase in area of integrated circuit elements within a bin, performing logic modifications within selected bins of the integrated circuit design to allow congestion of the placement to be improved.

12. A method of modifying an integrated circuit design to facilitate placement of circuit elements within one or more regions called bins on an integrated circuit design grid, comprising the steps of:

performing an initial placement of integrated circuit elements within bins on the design grid, connections between the integrated circuit elements being represented as nets within a netlist describing the integrated circuit design;

a2

calculating congestion of the initial placement; and

subject to limits on the increase in area of integrated circuit elements within a bin, performing logic modifications within selected bins of the integrated circuit design to allow congestion of the placement to be improved;

wherein the logic modifications improve timing of selected nets belonging to the selected bins, reducing constraints on a subsequent placement step.

15. A computer-readable medium including instructions for modifying an integrated circuit design to facilitate placement of circuit elements within one or more regions called bins on an integrated circuit design grid, including instructions for:

a3

performing an initial placement of integrated circuit elements within bins on the design grid;

calculating congestion of the initial placement; and

subject to limits on the increase in area of integrated circuit elements within a bin, performing logic modifications within selected bins of the integrated circuit design to allow congestion of the placement to be improved.

16. A computer-readable medium including instructions for modifying an integrated circuit design to facilitate placement of circuit elements within one or more regions called bins on an integrated circuit design grid, including instructions for:

performing an initial placement of integrated circuit elements within bins on the design grid, connections between the integrated circuit elements being represented as nets within a netlist describing the integrated circuit design;

calculating congestion of the initial placement; and

subject to limits on the increase in area of integrated circuit elements within a bin, performing logic modifications within selected bins of the integrated circuit design to allow congestion of the placement to be improved;

wherein the logic modifications improve timing of selected nets belonging to the selected bins, reducing constraints on a subsequent placement step.

17. Apparatus for modifying an integrated circuit design to facilitate placement of circuit elements within one or more regions called bins on an integrated circuit design grid, comprising:

means for performing an initial placement of integrated circuit elements within bins on the design grid;

means for calculating congestion of the initial placement; and

means for, subject to limits on the increase in area of integrated circuit elements within a bin, performing logic modifications within selected bins of the integrated circuit design to allow congestion of the placement to be improved.

18. Apparatus for modifying an integrated circuit design to facilitate placement of circuit elements within one or more regions called bins on an integrated circuit design grid, comprising:

means for performing an initial placement of integrated circuit elements within bins on the design grid, connections between the integrated circuit elements being represented as nets within a netlist describing the integrated circuit design;

means for calculating congestion of the initial placement; and

means, subject to limits on the increase in area of integrated circuit elements within a bin, performing logic modifications within selected bins of the integrated circuit design to allow congestion of the placement to be improved;

wherein the logic modifications improve timing of selected nets belonging to the selected bins, reducing constraints on a subsequent placement step.

REMARKS

By the present amendment, the claims would be amended to account for the possibility of performing the present invention using only a single bin (i.e., one encompassing the entire integrated circuit) as opposed to multiple bins. This change is not believed to affect patentability of the claims. Entry of the amendment is respectfully requested.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

By: _____
Michael J. Ure
Registration No. 33,089

P.O. Box 1404
Alexandria, Virginia 22313-1404
(650) 622-2300

Date: March 6, 2000

CERTIFICATE OF FACSIMILE TRANSMISSION

I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS BEING FACSIMILE TRANSMITTED TO THE PATENT AND TRADEMARK OFFICE ON THE DATE SHOWN BELOW.

Name of person signing certification: Sharon E. Byam

Date: March 7, 2000 Signature: Sharon E. Byam

Patent

Attorney's Docket No. 032260-004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)	
	)	
Sharad Malik, et al.	)	Group Art Unit: 2763
	)	
Application No.: 09/097,076	)	Examiner: Jones, H.
	)	
Filed: June 12, 1998	)	
	)	
For: METHOD FOR LOGIC OPTIMIZATION FOR IMPROVING TIMING AND CONGESTION DURING PLACEMENT IN INTEGRATED CIRCUIT DESIGN	)	

RECEIVED 3/7/00

OFFICIAL

AMENDMENT/REPLY TRANSMITTAL LETTER

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Enclosed is an Amendment for the above-identified patent application.

No additional claim fee is required.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

P.O. Box 1404
Alexandria, Virginia 22313-1404
(650) 622-2300

By: Michael J. Urbe
Registration No. 33,089

Date: March 7, 2000

(07/00)

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Name of porson signing certification: Sharon E. Byam

Date: March 7, 2000 Signature: Sharon E. Byam

Patent
Attorney's Docket No. 032260-004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)	**BOX AF**
	)	
Sharad Malik, et al.	)	Group Art Unit: 2763
	)	
Application No.: 09/097,076	)	Examiner: Jones, H.
	)	
Filed: June 12, 1998	)	
	)	
For: METHOD FOR LOGIC OPTIMIZATION FOR IMPROVING TIMING AND CONGESTION DURING PLACEMENT IN INTEGRATED CIRCUIT DESIGN	)	

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Assistant Commissioner for Patents
Washington, D.C. 20231

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1. A method of modifying an integrated circuit design to facilitate placement of circuit elements within one or more regions called bins on an integrated circuit design grid, comprising the steps of:

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Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

By: _____
Michael J. Ure
Registration No. 33,089

P.O. Box 1404
Alexandria, Virginia 22313-1404
(650) 622-2300

Date: March 6, 2000

APR-18-00 TUE 11:22 AM BU[illegible] DOANE SWECKER FAX NO. 6506[illegible]99 P. 01

BURNS DOANE SWECKER & MATHIS LLP

ALEXANDRIA, VIRGINIA
REDWOOD SHORES, CALIFORNIA
DURHAM, NORTH CAROLINA

REPLY TO:
SUITE 700
333 TWIN DOLPHIN DRIVE
REDWOOD SHORES, CA 94065

TELEPHONE: +1-650-622-2300
FACSIMILE: +1-650-622-2499

DATE: April 18, 2000

RECIPIENT INFORMATION		SENDER INFORMATION	
To:	Dr. Hugh Jones, Examiner Art Unit 2763, U.S. Patent & Trademark Office	From:	Michael J. Ure
Voice Tel. No.:	(703) 305-0023	Voice Tel. No.:	(650) 622-2325
Fax Tel. No.:	(703) 308-6306	Sent By:	Sharon Byam (650) 622-2417
Your Ref.:	Official	Our Ref.:	032260-004
		Total Pages (Incl. This Cover Page):	6

RE: USSN 09/097,076

MESSAGE: Following is the Amendment we spoke about on the telephone today.

RECEIVED 4-16-00

NOTE: The information contained in this facsimile message is attorney-client privileged and contains confidential information intended only for the use of the person(s) named above and others expressly authorized to receive it. If you are not the intended recipient, you are hereby notified that any dissemination, distribution or copying of this message is prohibited and you are asked to notify us immediately by telephone and to return this message to us by mail without copying it.

Any questions regarding compatibility should be directed to our Office Services Department at +1.703.836.6620.

(BDSM 3/99)

CERTIFICATE OF FACSIMILE TRANSMISSION

I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS BEING FACSIMILE TRANSMITTED TO THE PATENT AND TRADEMARK OFFICE ON THE DATE SHOWN BELOW.

Name of person signing certification: Sharon E. Byam

Date: March 7, 2000 Signature: Sharon E. Byam
Re-faxed April 18, 2000 Sharon E. Byam

Patent
Attorney's Docket No. 032260-004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)	
	)	
Sharad Malik, et al.	)	Group Art Unit: 2763
	)	
Application No.: 09/097,076	)	Examiner: Jones, H.
	)	
Filed: June 12, 1998	)	
	)	
For: METHOD FOR LOGIC OPTIMIZATION FOR IMPROVING TIMING AND CONGESTION DURING PLACEMENT IN INTEGRATED CIRCUIT DESIGN	)	Official

AMENDMENT/REPLY TRANSMITTAL LETTER

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Enclosed is an Amendment for the above-identified patent application.

No additional claim fee is required.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

P.O. Box 1404
Alexandria, Virginia 22313-1404
(650) 622-2300

By: _____
Michael J. Ure
Registration No. 33,089

Date: March 7, 2000

(02/00)

UNITED STATES L ...RTMENT OF COMMERCE
Patent andTrademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
09/097,076	06/12/98	MALIK S	032260-004

021839 LM02/0509
BURNS DOANE SWECKER & MATHIS
P O BOX 1404
ALEXANDRIA VA 22313-1404

EXAMINER	
JONES, H	
ART UNIT	**PAPER NUMBER**
2763	10

DATE MAILED: 05/09/00

Response to Rule 312 Communication

☐ The petition filed _____ under 37 CFR 1.312(b) is granted. The paper has been forwarded to the examiner for consideration on the merits.

_____

_____
Director,
Patent Examining Group _____

☑ The amendment filed 4/18/2000 under 37 CFR 1.312 has been considered, and has been:

☑ entered.

☐ entered as directed to matters of form not affecting the scope of the invention (Order 3311).

☐ disapproved. See explanation below.

☐ entered in part. See explanation below.

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER

FORM PTOL-271 (REV. 1/96)

★ U.S. GPO: 1996-404-498/40514

Paper # 11 is missing from the File History. Please see content sheet.

Please pardon any inconvenience.

B #1048

Patent
Attorney's Docket No. 032260-004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of)
)
Sharad Malik, et al.)
)
Application No.: 09/097,076)
)
Filed: June 12, 1998)
)
For: **METHOD FOR LOGIC OPTIMIZATION FOR IMPROVING TIMING AND CONGESTION DURING PLACEMENT IN INTEGRATED CIRCUIT DESIGN**)

FEB 2 5 2000

Attention: **DRAFTING BRANCH**

Group Art Unit: 2763

Examiner: Jones, H.

SUBMISSION OF FORMAL DRAWINGS

Assistant Commissioner for Patents
Washington, D.C. 20231

ATTN: OFFICIAL DRAFTSMAN

Sir:

Enclosed please find two sheets of formal drawings for review by the Patent and Trademark Office in connection with the Notice of Allowance mailed January 31, 2000. Should the enclosed drawings require changes, it is respectfully requested that the Patent and Trademark Office notify the undersigned of same.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

By: _____
Robert E. Krebs, Esq.
Registration No. 28,885

P.O. Box 1404
Alexandria, Virginia 22313-1404
(650) 622-2300

Date: February 28, 2000

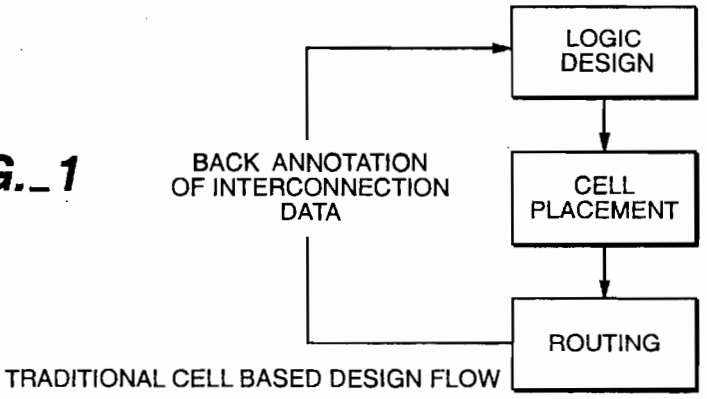
(09/99)

09/097,076

032260-004

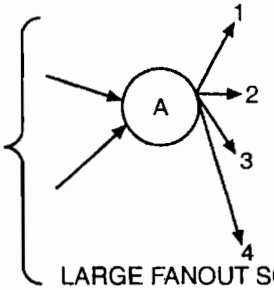
6192508 1 / 2

FIG._1



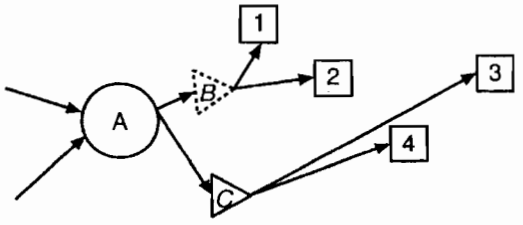
TRADITIONAL CELL BASED DESIGN FLOW

FIG._3A



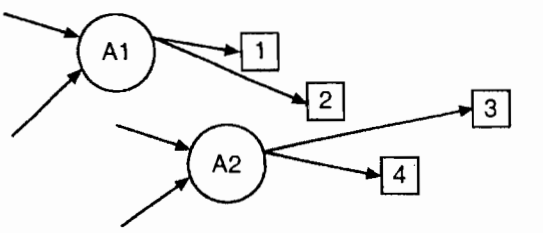
LARGE FANOUT SOURCE OF CONGESTION

FIG._3B



FANOUT SPLITTING USING BUFFERING

FIG._3C



FANOUT SPLITTING USING NODE SPLITTING

032260-004

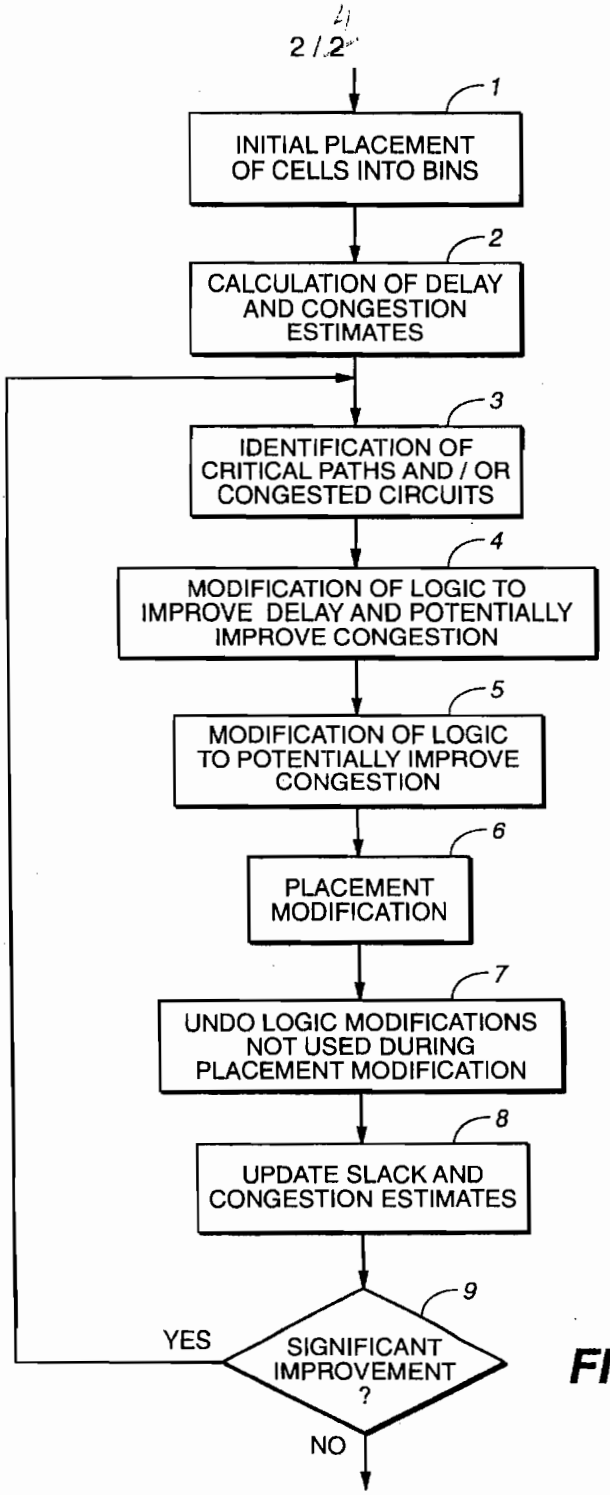
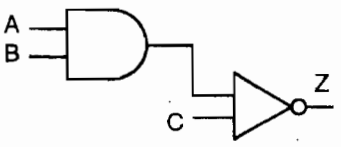


FIG._2

032260-004

3 / 4



BOTH GATES ARE IN THE SAME BIN

FIG._4A

FIG._4B

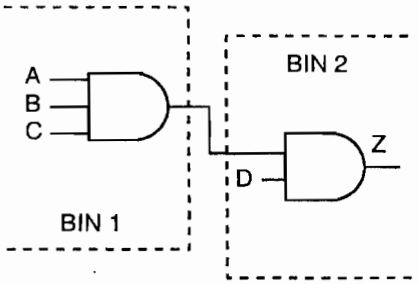


FIG._5A

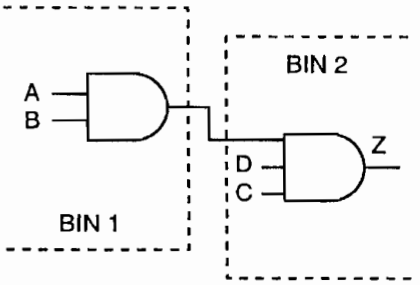


FIG._5B

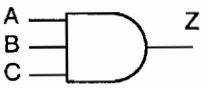


FIG._6A

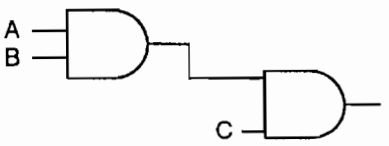


FIG._6B

4/4

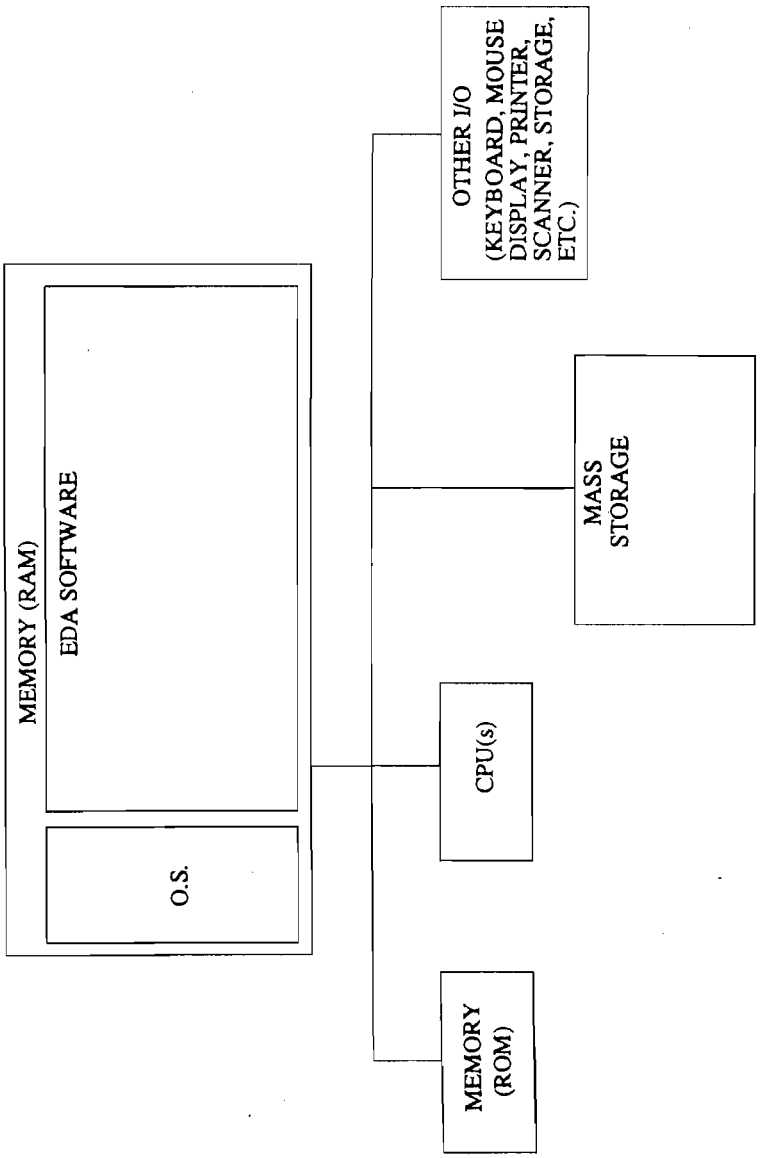

MEMORY (RAM)
EDA SOFTWARE
O.S.
CPU(s)
MEMORY (ROM)
MASS STORAGE
OTHER I/O (KEYBOARD, MOUSE DISPLAY, PRINTER, SCANNER, STORAGE, ETC.)

Fig. 7

#13

Patent
Attorney's Docket No. 032260-004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	Attention: **DRAFTING BRANCH**
MALIK et al.	Allowed: January 31, 2000
Application No.: 09/097,076	Batch: H44
Filed: June 12, 1998	Group Art Unit: 2763
For: METHOD FOR LOGIC OPTIMIZATION FOR IMPROVING TIMING AND CONGESTION DURING PLACEMENT IN INTEGRATED CIRCUIT DESIGN	Examiner: Patricia A. Small

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Sir:

For review by the Patent and Trademark Office in connection with the above-noted application, enclosed please find one sheet of formal drawings comprising Figures 4A, 4B, 5A, 5B, 6A and 6B Should the enclosed drawings require changes, it is respectfully requested that the Patent and Trademark Office immediately notify the undersigned of same.

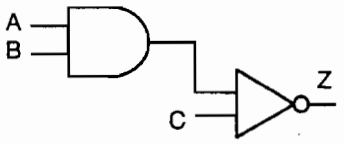
Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

By: _____
Robert E. Krebs
Registration No. 25,885

P.O. Box 1404
Alexandria, Virginia 22313-1404
(650)622-2300
Date: November 21, 2000

(10/00)



BOTH GATES ARE IN THE SAME BIN

FIG._4A

FIG._4B

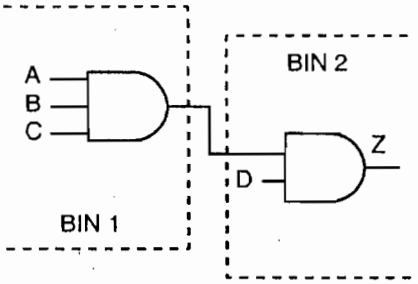


FIG._5A

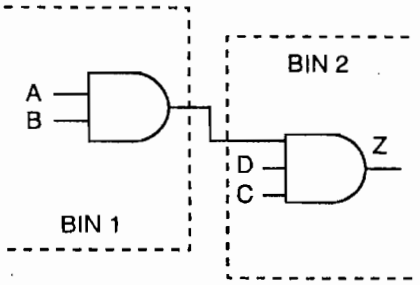


FIG._5B

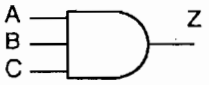


FIG._6A

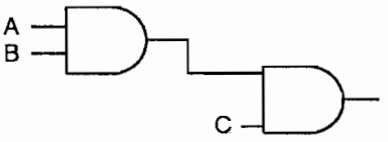


FIG._6B

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Patent
Attorney's Docket No. 032260-004

#14
#15

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)	Attention: **EXAMINER JONES**
MALIK et al.	)	Allowed: January 31, 2000
Application No.: 09/097,076	)	Batch: H44
Filed: June 12, 1998	)	Group Art Unit: 2763
For: METHOD FOR LOGIC OPTIMIZATION FOR IMPROVING TIMING AND CONGESTION DURING PLACEMENT IN INTEGRATED CIRCUIT DESIGN	)	Examiner: H. Jones

COMMUNICATION

Assistant Commissioner for Patents
Washington, D.C. 20231

Examiner Jones:

In accordance with the telephonic conversation of December 7, 2000 with Robert E. Krebs, Esq., enclosed are formal drawings comprising Figures 4A, 4B, 5A, 5B, 6A, 6B and 7 for the subject application. Also enclosed is a duplicate of the submission of formal drawings, filed with the U.S.P.T.O. on November 22, 2000.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

By: _____
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Registration No. 25,885

P.O. Box 1404
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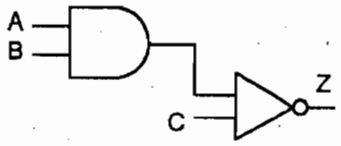
Date: December 7, 2000

(10/00)



BOTH GATES ARE IN THE SAME BIN

FIG._4A

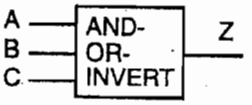


FIG._4B

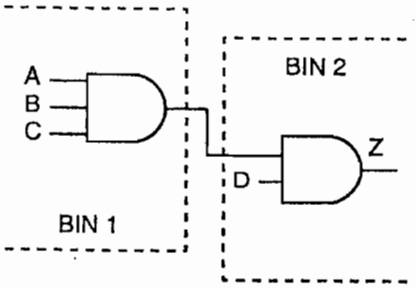


FIG._5A

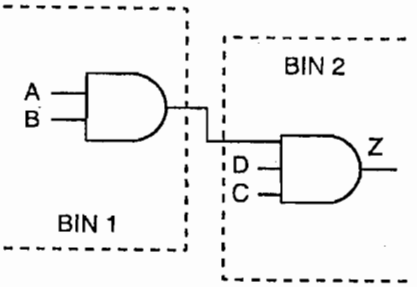


FIG._5B

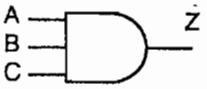


FIG._6A

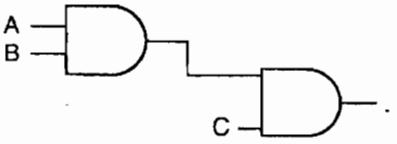


FIG._6B

TAB 25

Physical Hierarchy Generation with Routing Congestion Control

Chin-Chih Chang*, Jason Cong*, Zhigang (David) Pan†, and Xin Yuan*

ABSTRACT

In this paper, we develop a multi-level physical hierarchy generation (mPG) algorithm integrated with fast incremental global routing for directly updating and optimizing congestion cost during placement. The fast global routing is achieved by using a fast two-bend routing and incremental A-tree algorithm. The routing congestion is modeled by the wire usage estimated by the fast global router. A hierarchical area density control is also developed for placing objects with significant size variations. Experimental results show that, compared to GORDIAN-L , the wire length driven mPG is 3 – 6.5 times faster and generates slightly better wire length for test circuits larger than 100K cells. Moreover, the congestion driven mPG improves 50% wiring overflow with 5% larger bounding box wire length but 3 – 6% shorter routing wire length measured by graph based A-tree.

Categories and Subject Descriptors

B.7.2 [**Hardware**]: INTEGRATED CIRCUITS—*Design Aids*

General Terms

Algorithms, Design, Experimentation, Performance

Keywords

Placement, routing, congestion, interconnect, physical hierarchy, deep sub-micron

1. INTRODUCTION

Interconnect has become the dominating factor in determining overall system performance and reliability. Inevitably, it impacts *all* stages of the design flow. In [1], Cong proposed a three phase interconnect-centric design flow, including (1) interconnect planning, (2) interconnect synthesis, and (3) interconnect layout in order to emphasize interconnect planning and optimization throughout the entire design process.

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ISPD'02, April 7-10, 2002, San Diego, California, USA.
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	Total Wire Length (meter)						all	net
layers	M1	M2	M3	M4	M5	M6	layers	count
nets <0.5mm	0.04	1.36	2.08	1.41	0.17	0.00	4.1%	43.2%
nets [0.5-5mm]	0.22	4.51	11.81	20.57	12.22	6.83	45.7%	48.7%
nets >5mm	0.01	0.26	2.93	14.43	20.87	23.11	50.2%	8.1%
all nets	0.2%	5.0%	13.7%	29.6%	27.1%	24.4%	100%	100%

Table 1: Wire length distribution on all routing layers of the block level net list of a micro-processor design

The interconnect planning phase is particularly important because it provides early assessments on the system performance thereby enabling performance optimization in the early design stages. In addition to performance optimization, it is equally important to reduce design uncertainty and ensure that the planned results can be realized in the later design stages without significant deviations.

An important step in interconnect planning is *physical hierarchy generation.* There are some recent studies on generating good physical hierarchy from the flattened function and logic hierarchy for performance optimization [2, 3]. However, they have little or no consideration of routing congestion, which may cause uncertainty in later design stages because the planned global interconnects in overly congested areas may be forced to make detours or change layers.

The fact that more routing layers are added in the VLSI design suggests that the global interconnect congestion problem is worsening. Table 1 shows the wire length distribution based on the block level net list of a leading high performance microprocessor design from Intel [4], which demonstrates the congestion problem in global interconnects. The data show that over 95% of the wires are from wires longer than $0.5mm$ and over 80% of the wires are on the top three layers. It shows that there is high resource competition among long global interconnects on those top layers (which provide faster connections). Since long wires are usually sized wider for better performance, the top layers are much more congested.

The above data suggest that the performance estimation in the interconnect planning must consider layer assignment and congestion in global interconnects.

Several existing works consider the congestion during placement or floorplan. In [5, 6], it is shown that there is a mismatch between wire length and congestion objectives. In [7], a simple LZ-shape routing is incorporated into a simulated annealing based floorplanning engine to consider congestion. However, there may not be enough global interconnects seen by a floorplanner. In [8], the wiring demand of a net is modeled by a weighted bounding box length. The wiring demand estimation can be fast, though it may

be inaccurate. In [9], pre-computed Steiner tree topologies on a few grid structures are used for wiring demand estimations. This approach is tailored for recursive partition placement and may not foresee congestion problems within each partition. In [10, 11, 12], an indirect cell padding or region growing/shrinking is applied to the placement after congestion analysis. This type of approach will not dynamically monitor the congestion changes and has less control on reducing congestion. In [13], a post-processing of moving cells with Steiner tree reconstructions is used. In this approach, the cell movement is limited and reconstructing the Steiner trees on each movement is too expensive. In [14], it is shown that a post-processing technique is effective in minimizing congestion because routing congestion correlates with wire length in a global view. In [15], a post-processing with a new congestion model is proposed. The congestion is first estimated by the method in [8] and revised by expanding certain congestion regions (by solving an integer programming problem). This approach improves the accuracy of congestion but the routing congestion is still not dynamically updated.

In general, the most accurate congestion estimation still comes from the global router itself. However, due to the high computational complexity, most previous works used a variety of simplified approximations to estimate the congestion. Our approach differs from the others by building a fast global router and integrating it with an efficient multi-level placement engine to provide dynamic routing congestion guidance to the placement engine.

2. PROBLEM FORMULATION

The interconnects of a VLSI circuit are determined by (1) the locations and sizes of logic gates, flip-flops, and buffers; (2) the interconnect geometry that includes wire locations, layers, and widths. Although interconnect delay is the dominating factor in system performance, only the delays of "long" interconnects are sensitive to wiring geometry. The delays of "short" interconnects are determined mainly by the driver/receiver sizes and are less sensitive to wiring geometry. It is an important problem of identifying and optimizing global interconnects in early design stages. This important problem of determining global interconnects can be solved by physical hierarchy generation.

The physical hierarchy is represented by a bin structure and cell location assignment. We can use the bin centers to roughly specify cell locations. Global routing can be performed to estimate net topologies. The finer the bin structure becomes, the more accurate the cell locations and net topologies. We also call our physical hierarchy generation process "coarse placement" because we only place cells in coarse locations (bin centers).

The inputs of the physical hierarchy generation consist of logic hierarchy, design specification, and technology. The logic hierarchy includes a hierarchical net list description consisting of library cells, hard intellectual property (IP) blocks, and soft IP blocks. The width, height, and delay information of library cells and hard IPs are known. The soft IP blocks can be further flattened into other hard IP blocks or library cells.

Given the above inputs, the physical hierarchy generation places cells in a bin structure for optimizing the design objectives (delay, area, etc.). The outputs include: (1) block locations, specified by bin centers; (2) global nets (inter-bin nets) routing estimations (topology, wire sizing, and layer assignments); (3) delay estimations, power estimations, etc.

In this paper, we will only focus on the wire length minimization and routing congestion minimization.

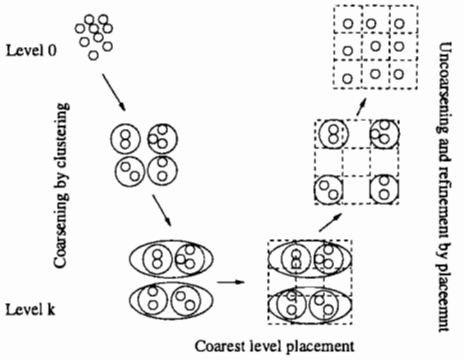

Figure 1: V-shape multi-level simulated annealing coarse placement framework

3. PHYSICAL HIERARCHY GENERATION

High computational complexity is the major challenge for physical hierarchy generation. Inspired by the recent success of the multi-level methods in efficiently handling high complexity designs in the VLSI CAD area [16, 17, 18], the backbone of our system is a multi-level simulated annealing (SA) engine.

3.1 Overview

Figure 1 shows an overview of our multi-level coarse placement framework. It includes a coarsening phase which recursively builds coarsening levels and a refinement phase which refines each coarser level representation to obtain a finer level representation. Our coarsening is done by iterative clustering. We select the *FirstChoice* (FC) clustering algorithm [19] because it experimentally gives us better clustering for coarse placement.

Our refinement is done by a simulated annealing (SA) based placement engine which places each cluster in the current level in a placement bin. We choose to use an SA based placement as in [20, 21] for the flexibility of integrating various design objectives and constraints. We use the *same* placement bin structure for each level.

For each refinement of a coarser level solution, the SA engine moves clusters of the current level (after declustering from the coarser level solution) to optimize bounding box wire length or routing congestion cost, both under area density constraints. The area density constraints are enforced by a hierarchical area density control algorithm. The routing congestion is evaluated by using a fast global router. The details of our algorithms shall be discussed in subsequent sections.

3.2 Hierarchical Area Density Control

Each placement bin has an area bound which is the area that can be used for cells placed in this bin. If the total area of the cells placed in a bin exceeds its area bound, some cells need to be moved to other locations. If the area bound in each placement bin is strictly enforced, a coarse placement solution can be legalized to an overlap-free detailed placement solution without moving any cell out of the placement bin assigned by the coarse placement.

It is difficult, however, to maintain strict area bound in each placement bin during the placement process. The conventional wisdom is to allow some area overflow up to a fixed percentage of the bin area bounds such that a detailed placement solution can be obtained without significant cell movement.

The fixed overflow percentage does not work well in a multi-

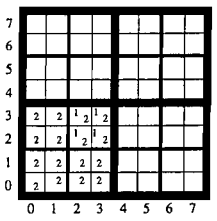

Figure 2: Bin hierarchy for area density control

level coarse placement due to the significant variances in cluster sizes. The clusters in coarser levels may even be larger than a placement bin. One solution is to use coarser bin structures in coarser levels, however, it looses the accuracy and creates cost jumps when switching to finer bin structures.

We solve this problem by a hierarchical area density control algorithm. Our density control imposes a hierarchy of bin structures on the target bin structure and enforces relaxed area constraints for all the bins in the hierarchy. Subsequently we shall show that the area constraints are gradually tighten in our multi-level framework while allowing more freedom for cluster moves.

The bin hierarchy is formed by recursively grouping adjacent bins to generate the bins in next level. Figure 2 shows an example of a bin hierarchy where boundary lines of different levels of the bin structure are drawn differently. In this figure, there are three bin structures: an 8×8 bin structure at level 0, a 4×4 bin structure at level 1, and a 2×2 bin structure at level 2.

Denote A_b^i as the area bound for a bin B_b^i in level i, which is also the summation of all area bounds of the level 0 bins contained in B_b^i. Similarly, denote U_b^i as the current area usage U_b^i for bin B_b^i, which is also the summation of all current area usages of the level 0 bins contained in B_b^i. The hierarchical area constraints are enforced on each cluster move. For a cluster move that moves a cluster c of area a_c to a bin B_b^0, for any bin $B_{x_i}^i$ on level i that contains the bin B_b^0, the overflow of bin $B_{x_i}^i$ must be smaller than ka_c, where $k \geq 1$ is a user specified parameter ($\forall i(U_{x_i}^i + a_c - A_{x_i}^i) \leq ka_c$).

For example, if a cluster with area a_c is moved to bin $(2,3)$ in Figure 2, the area constraints of the following bins are enforced: bin $(2,3)$ on level 0, the level 1 bin covering the region marked with 1 in Figure 2, and the level 2 bin marked with 2 in Figure 2.

Using the hierarchical area density control, our placement engine can place clusters with mixed sizes. We will legalize macro cell locations after a few levels from the coarsest levels. As the refinement processes continue, the area constraints will be gradually tightened because the clusters become smaller. By using this method, our annealing engine can efficiently handle mixes of big and small modules and will not be stuck due to area constraints.

If the area constraint is satisfied in a region, by applying the pigeon hole principle, at least one of the sub-regions of the region satisfies the area constraint. We apply this property in our move selection. If the SA engine generates a target location that moves a cell to a location that violates the hierarchical area constraints, we can efficiently find an alternative location. We can first find the smallest bin B in our hierarchy that contains the target location and all the higher level bins that contain this bin also satisfies the area constraint. An alternative location can be found by recursively applies the pigeon hole principle from this bin B.

3.3 Global Interconnect Topology Generation and Layer Assignment

Since most of the nets are two-pin nets and a multi-pin net can be decomposed into two-pins nets, we first build a fast, congestion avoidance two-bend router (LZ-router) for two-pin nets. We will use this fast two-pin net routing algorithm with an incremental A-tree generation algorithm for multi-pin nets to build a fast global router.

The fast global router also includes a fast layer assignment algorithm which assigns nets according to net criticality. More critical nets have higher priority to choose better routing layers and routing topologies satisfying the performance constraints.

The layer assignment is not performed on each SA move in order to save the run time. In our implementation, we only perform layer assignment at the beginning of each SA phase that refines a placement solution from a coarser level to obtain a finer level placement solution.

3.3.1 *Routing for Two-pin Nets*

We use a fast two-bend routing algorithm to route two-pin nets, with at most two bends. We call the two-bend routing "LZ-routing" and our two-bend router an "LZ-router."

The possible number of configurations of LZ-routing that connects two pins with coordinates (i,j) and $(i+x, i+y)$ is $\mid x \mid + \mid y \mid$. However, with a simple minded implementation, finding an LZ-route requires to calculate $\mid x \mid \times \mid y \mid$ wire usage queries on bin boundaries, which is still quite expensive.

Our LZ-router uses auxiliary data structures (similar to a segment-tree data structure) to find good quality routes by performing a binary search of the possible routes for a two-pin net. For two pins bounded by a rectangle bounding box B, our LZ-router first measures congestion of B and its boundaries on both the horizontal and vertical layer to determine whether horizontal-vertical-horizontal (HVH) routing or vertical-horizontal-vertical (VHV) routing is less congested and should be used.

Assuming we are using VHV routing, our algorithm recursively makes a horizontal cut on B and selects the one with a smaller average density to route. It stops when the choice narrows to a single row.

If the complexity for a region query is R, the complexity of our LZ-router is $O(log(\mid x \mid + \mid y \mid)R)$ because it takes at most $O(log(\mid x \mid + \mid y \mid))$ binary search steps to find a route. Given a $g_x \times g_y$ bin structure, any region query used in our LZ-router can be (approximately) answered in $O(log(g_x + g_y))$ using segment-tree-like data structures. Therefore, the complexity for our LZ-routing is $O(log(\mid x \mid + \mid y \mid)log(g_x + g_y))$.

THEOREM 1. *Given a $g_x \times g_y$ bin structure, the complexity for the LZ-router to route two pins with coordinates (i,j) and $(i+x, j+y)$ is $O(log(\mid x \mid + \mid y \mid)log(g_x + g_y))$.*

Due to page limitations, the details of the auxiliary data structures, the complexity analysis, and the proof are omitted. They can be found in the technical report [22].

3.3.2 *Incremental Hierarchical A-tree Construction*

For a multi-pin net, we would like to construct a rectilinear Steiner arborescence tree (A-tree) for our routing estimation. A rectilinear Steiner arborescence tree (A-tree) is a shortest path rectilinear Steiner tree. There are some heuristics that can construct an n-pin A-tree in $O(n \log n)$ time with a solution no worse than 2x the optimal A-tree solution, e.g., [23, 24]. However, if we reconstruct each A-tree for any of the pin location updates, we may spend $O(n^2 \log n)$ for each n-pin net on a pass of moving all clusters, which is too expensive.

We propose an incremental A-tree (IncA-tree) algorithm that can be efficiently updated. We only explain the construction in the first

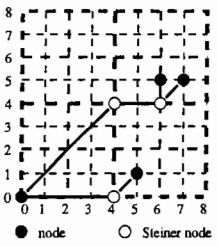

Figure 3: An example of IncA-tree

quadrant because the construction in all quadrants is similar. Given a grid structure consisting of $(2^m+1) \times (2^m+1)$ grids on the first quadrant, we can recursively perform quad-partitioning on the grid structure until it reaches the unit grid.

The lower-left corner of the partition is the root for a subtree connecting all the pins inside this partition. By recursively performing such quad-partitioning, we can build an A-tree such that each pin at location (x, y) can connect to the origin $(0, 0)$ with $max(\log x, \log y)$ edges. Therefore, any pin insertion (deletion) to location (x, y) only incurs at the most $\log(x + y)$ edge insertions (deletions). Therefore, each operation of moving a pin from (x_1, y_1) to (x_2, y_2) incurs at the most $\log(x_1 + y_1) + \log(x_2 + y_2)$ edge changes. An example of an IncA-tree is shown in Figure 3.

With the fast two-pin routing and incremental A-tree routing, for an n-pin net with bounding box length L on a $g_x \times g_y$ bin structure, the complexity for updating a non-root pin move is $O(\log L)$ times the complexity of LZ-routes $O(\log L \log(g_x + g_y))$, which is $O(\log L^2 \log(g_x + g_y))$. For moving the root, the complexity is $O(n \log^2 L \log(g_x + g_y))$. While providing superior guidance for congestion optimization during coarse placement, the run time overhead of our congestion cost updating grows slowly due to the low logarithmic complexity.

3.4 Multi-level Simulated Annealing Coarse Placement

The details of the SA engine is described below.

3.4.1 Solution Space:

The *same* bin structure is used for placement on each level. Clusters are placed at bin centers subject to hierarchical area constraints, which is explained in Section 3.2.

3.4.2 Cost Function:

The cost function for our SA engine has two modes: wire length driven and congestion driven. The cost function for the wire length driven mode is the simple summation of all the bounding box wire lengths of all nets.

The fast global router described in Section 3.3 is used to estimate the wire usage in each bin. The cost function for the congestion driven mode is the quadratic sum of the wire usages of all routing layers of all bins. This cost is equivalent to the sum of weighted wire length by weighting all the wire segments in each bin by the wire usage of that bin.

This cost function encourages the SA moves that result in shorter wire length and less congestion. This cost function can also be efficiently updated if the wire usage is stored by a segment-tree-like data structure.

Because minimizing wire length is strongly related to congestion minimization, we will run our multi-level SA coarse placement with wire length minimization on coarser levels. We only turn on the congestion optimization at the last few finest levels of optimization. We have a "reduced mode" that only turns on the congestion driven at the finest level when the accepting ratio is lower than a predefined threshold t_r and alternatively runs the congestion driven and wire length driven modes with a fraction of congestion driven runs, denoted as f_c. Our experiments find that $t_r = 0.075$ and $f_c = 80\%$ gives best tradeoff of run time and solution quality.

3.4.3 Neighborhood Structure:

Two moves are used (1) cluster move; (2) I/O pads swap (not used in the experiments of this paper). A cluster move randomly selects a cluster and moves it to another bin. The target location is either randomly generated (within some range limit) or computed to optimize bounding box wire length. The experimental setting of random moves probability is $max(accept\ ratio, 0.6)$. If the generated move violates area constraints, an alternative target location is generated according to the method described in Section 3.2.

3.4.4 Cooling Schedule:

Let n_i be the number of clusters of level i. The cooling schedule is shown below.

- **starting temperature:** The starting temperature for the coarsest level (level k) is calculated by 20 times of the standard deviation of the costs of n_k random moves as suggested by [25]. For level i ($i < k$), it is calculated by binary searching to find the temperature with the expected cost-change of n_i moves close to zero [26].
- **next temperature calculation:** The next temperature calculation is a function of accepting ratio α. For a given temperature T, the next temperature is $0.5T$ if $\alpha > 0.96$; $0.9T$ if $0.8 < \alpha \leq 0.96$; $0.95T$ if $0.15 < \alpha \leq 0.8$; $0.8T$ if $\alpha \leq 0.15$.
- **inner number:** We use two inner numbers $inner_0$ and $inner_1$. For each temperature on level i, we first start a pass with $inner_0 \times n_i$ moves. If the current pass reduces the total cost, the temperature is repeated with $inner_1 \times n_i$ moves until m cost increase passes are encountered. The values set experimentally are: $inner_0 = 1$, $inner_1 = 5$, and $m = 2$.
- **freezing temperature:** The freezing temperature is computed by $\lambda C/ec$, where C is the current cost; λ is a user input parameter; ec is the net count of the current level. The default value for λ is 0.005.

4. EXPERIMENTAL RESULTS

Our physical hierarchy generation algorithm is implemented in C++/STL. It can be run with three modes: wire length minimization (mPG), congestion cost driven at the finest level (mPG-cg), and the "reduced mode" described in Section *3.4.2* (mPG-cg.rd). Our experiments are conducted on a Sun Blade 1000 workstation running at 750MHz frequency (except the experiments done in Section 4.4).

We obtained our benchmark circuits from different sources: [17], [27], and industrial benchmarks from IBM. [1]

For the wire length comparisons, we use circuits in [17] such that we can compare to [17] and GORDIAN-L [29]. We do not use circuits from [27] because GORDIAN-L can not produce results for some circuits probably due no connections to I/O pads caused by

[1] Please note that although both [17] and [27] have circuits derived from ISPD98 IBM benchmark suit [28], they are not the same. We rename the circuits in [17] by adding "-p" suffixes to indicate the differences. The circuits in [17] have the same net lists as in [28], however, all the cells have the same size. The circuits in [27] use the cell sizes specified in [28], however, all the big macro cells together with all the nets connecting to them are removed, thus most of the circuits do not have connections to I/O pads.

circuit	#cells	#nets	Gor+Dom		mPG+Dom	
			WL (10^6)	CPU (s)	WL (10^6)	CPU (s)
avqsmall	21854	22124	11.3	857	11.5 (1.02)	694 (0.81)
avqlarge	25114	25384	12.6	925	12.0 (0.95)	764 (0.83)
ibm04-p	27220	31970	6.86	1577	6.59 (0.96)	1397 (0.89)
ibm07-p	45639	48117	10.9	4385	10.3 (0.94)	3434 (0.78)
ibm09-p	53110	60902	11.8	6767	11.6 (0.98)	3364 (0.50)
ibm10-p	68685	75196	18.8	14133	18.9 (1.01)	5526 (0.39)
ibm14-p	147088	152772	40.8	39657	38.8 (0.95)	13131 (0.33)
ibm15-p	161187	186608	52.1	63876	51.7 (0.99)	16091 (0.25)
ibm16-p	182980	190048	55.0	81868	51.5 (0.94)	19979 (0.24)
ibm17-p	184752	189581	67.9	98440	66.2 (0.97)	22281 (0.23)
ibm18-p	210341	201917	53.7	129065	50.0 (0.93)	19944 (0.15)

Table 2: Wirelength comparison with GORDIAN-L

circuit	nets characteristics					#moves	eva. time (s)		speed
	#nets	3pin	4pin	5pin	6^+pin		IncA	A-tree	up
ibm01-r	5681	36%	18%	14%	32%	12028	15.35	80.24	5.2X
ibm02-r	8506	20%	22%	23%	35%	19062	26.36	170.74	6.47X
ibm03-r	8137	38%	16%	11%	35%	21879	24.18	174.79	7.20X
ibm04-r	10580	37%	16%	13%	34%	26332	37.83	462.69	12.23X
ibm05-r	10433	11%	0%	23%	66%	28146	60.84	586.87	9.65X
ibm06-r	13968	28%	23%	14%	35%	32018	55.48	623.26	11.23X

Table 3: Congestion evaluation time comparison. Two-pin nets are removed.

big modules removals. For the congestion driven experiments, we use circuits in [27]. We do not use circuits in [17] because all the cells have the same area is not reasonable for routing.

4.1 Wirelength Comparison with GORDIAN-L

We compared our wirelength-driven mPG with GORDIAN-L [29] followed by DOMINO [30] on two of the largest circuits (*avqsmall, avqlarge*) in 1993 MCNC layout benchmark sets and the ISPD98 IBM benchmark suit offered by the authors of [17] in Table 2. We ran GORDIAN-L followed by DOMINO and reported the BBOX wirelength of the detailed placement results and total runtime in columns titled "Gor+Dom." Also we ran mPG followed by DOMINO and reported the wirelength and total runtime in columns titled "mPG+Dom" and listed the ratio between the wirelength and runtime of mPG and that of GORDIAN-L in parentheses.

It shows that mPG provides a slightly shorter wirelength and significant less run time, especially in circuits larger than 100K.

4.2 Speed-up by Incremental A-tree

The incremental A-tree algorithm enables us to directly integrate a global router into the placement engine without suffering from an overly-long runtime.

In this section, we shall provide the run time comparison between IncA-tree and an implementation that completely routes a net by an A-tree algorithm [23] whenever a pin of this net is moved during the simulated annealing process.

We used some circuits from IBM-PLACE benchmarks suite[27] for this experiment. For each circuit, we first eliminated all the two-pin nets and only kept the multi-terminal nets for testing.[2] For a move generated by SA engine, we used the IncA-tree algorithm to incrementally evaluate the congestion and recorded the runtime for a pre-determined number of moves. The identical set of moves were also evaluated by the A-tree algorithm.

It can be seen in Table 3 that the IncA-tree algorithm can speed up the evaluation process by a factor of at least 5 and even more when the nets with a higher degree become dominant.

[2] We use suffixes "-r" in the circuit names to indicate the two-pin nets are removed from [27].

4.3 Congestion Control Comparison

In order to evaluate effects of the congestion optimization, we implemented a global router based on the GA-tree algorithm [24] to evaluate the congestion of a placement solution. When constructing an A-tree topology for a net, the GA-tree algorithm can consider both the congestion and the obstacle information. It works on a routing graph where nodes represent routing bins and edges correspond to the shared boundaries of adjacent bins.

We can obtain a global routing solution with congestion control by using a slope-based cost function for edge weight to penalize the overflowed/highly congested edges (similar to that used in [31]) and updating the weight after routing each net.

The benchmarks for testing congestion control are chosen from the IBM-PLACE benchmarks suite [27].[3] For each test case, we ran GORDIAN-L followed by DOMINO to get a wirelength-driven placement result and then used our GA-tree based global router to evaluate the congestion. Meanwhile we ran mPG to perform wirelength-driven placement and ran mPG-cg and mPG-cg.rd to perform a congestion-driven placement. All mPG runs used the GA-tree based global router to evaluate the results. For all the test cases, we used two routing layers for global routing evaluation.

In Table 4, we reported the congestion pictures in total overflow (tot. ov), the maximal boundary congestion (max. b.cg), the routing wirelength (routing WL) and total bounding box wirelength for GORDIAN-L/DOMINO (G/D), mPG, mPG-cg, and mPG-cg.rd.

It can be seen that although in terms of bounding box wirelength, wirelength-driven placers (mPG and GORDIAN-L) offer better results in general, their routed wirelength actually becomes larger than that generated by mPG-cg on average. This implies that the bounding box wirelength is no longer a good metric for routability. A similar conclusion was also drawn in [15]. Meanwhile, the mPG-cg reduces any existing total overflow by 53–79% on average and reduces either the routed wirelength or the maximal boundary congestion, demonstrating that the congestion control done in the placement phase can benefit the routing phase. It is also shown that by properly placing the modules/blocks/cells in the placement phase, good interconnect planning can be carried out in the routing phase. The results of mPG-cg with the reduced mode demonstrate the tradeoff between runtime and solution-quality.

4.4 Experiments on Industrial Circuits

We also ran our program on 5 IBM test circuits (named ind1 to ind5, to avoid name confusion with the published IBM benchmark used in the previous section) on a Sun workstation running at 400MHz frequency, followed by IBM's in-house legalization and routing tools. These circuits use IBM ASIC standard cell libraries, with feature size from $0.15\mu m$ to $0.25\mu m$, and some circuits have a number of pre-placed macros (not counted in the cell number).

Table 5 shows the number of placeable cells (#cell), the number of nets (#nets), the grid size, the comparison of routed wirelength, maximum congestion, the number of overflowed edges and the number of nets that overflow.[4] It confirms that the placement results generated by mPG-cg have less congestion than that by mPG, with fewer congested edges and nets, though running much slower. The reduced mode mPG-cg.rd provides a tradeoff between run time and quality of result.

5. CONCLUSIONS

We presented a multi-level simulated annealing physical hierarchy generation algorithm (mPG-cg) integrated with incremental

[3] We removed the dangling cells in the circuits.

[4] The IBM tool reports the number of overflowed edges, not the total overflow.

circuit name	#cells	#nets	grid size	BBOX WL				routing WL				max. b.cg				tot. ov				CPU (s)			
				G/D	mPG	mPG -cg.rd	mPG -cg	G/D	mPG	mPG -cg.rd	mPG -cg	G/D	mPG	mPG -cg.rd	mPG -cg	G/D	mPG	mPG -cg.rd	mPG -cg	G/D	mPG	mPG -cg.rd	mPG -cg
ibm01	12028	11507	32×64	4.95e6	4.37e6	4.66e6	4.77e6	6.19e6	5.37e6	5.26e6	5.14e6	1.36	1.27	1.10	1.06	2284	950	319	114	1363	578	3133	8295
ibm04	26332	26163	64×64	1.70e7	1.66e7	1.74e7	1.73e7	1.96e7	1.97e7	1.96e7	1.87e7	1.20	1.26	1.22	1.06	1949	1266	639	77	3173	1228	9709	27922
ibm07	44811	44394	64×64	4.25e7	3.18e7	3.31e7	3.33e7	6.47e7	4.57e7	4.48e7	4.33e7	2.40	1.78	1.78	1.69	2.97e5	7.51e4	6.39e4	4.74e4	65027	2410	14683	43618
ibm11	68046	67016	64×64	-	4.19e7	4.37e7	4.36e7	-	4.85e7	4.78e7	4.59e7	-	1.25	1.10	1.02	-	3014	811	271	-	3440	17923	72010
ibm13	83806	80906	64×128	-	5.14e7	5.36e7	5.41e7	-	7.31e7	6.82e7	6.40e7	-	1.51	1.39	1.31	-	7.43e4	3.62e4	2.10e4	-	4393	27312	76768
ibm15	161196	157806	128×128	-	1.47e8	1.52e8	1.52e8	-	1.82e8	1.77e8	1.67e8	-	1.14	1.10	1.07	-	3971	1596	288	-	13285	74458	263706
avg.				-	1	1.05	1.05	-	1	0.97	0.94	-	1	0.93	0.87	-	1	0.47	0.21	-	1	6.1	18.9

Table 4: Congestion control comparison between wirelength-driven placement and mPG-cg.

circuit	#cell	#net	grid size	routed WL			max. cg			#edge-ov			#nets-ov			cpu(s)		
				mPG	mPG -cg.rd	mPG -cg	mPG	mPG -cg.rd	mPG -cg	mPG	mPG -cg.rd	mPG -cg	mPG	mPG -cg.rd	mPG -cg	mPG	mPG -cg.rd	mPG -cg
ind1	1099	1179	8×8	113	112	101	1.0	1.0	1.0	0	0	0	0	0	0	57	147	739
ind2	30997	32027	64×32	5520	5494	5369	1.1	1.1	1.1	1014	754	426	3608	3096	2566	1927	10247	40642
ind3	72940	73386	64×64	11601	11940	11863	1.3	1.1	1.03	9	3	1	133	57	24	5722	18527	59340
ind4	141862	153708	128×128	180094	180998	179473	2.53	2.53	2.53	5255	4783	4315	2809	2798	2634	58929	128036	361480
ind5	216111	221133	128×128	69545	69362	69188	1.7	1.7	1.7	1396	1310	1145	724	652	629	38773	92109	288096

Table 5: IBM circuit results.

A-tree algorithm and fast LZ-routing for fast congestion evaluation and optimization. Our placement engine also has a hierarchical area density control which allows us to place both mixed big and small clusters. Our experiments show that our mPG program is both competitive in wire length and run time. The congestion driven mPG (mPG-cg) can significantly reduce routing congestion.

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